

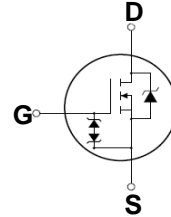
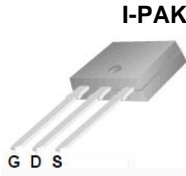
Features

- Low gate charge
- 100% avalanche tested
- Improved dv/dt capability
- Halogen free package
- JEDEC Qualification
- Improved ESD performance

$$V_{DSS} = 440 \text{ V @ } T_{jmax}$$

$$I_D = 3.4 \text{ A}$$

$$R_{DS(on)} = 1.6 \text{ } \Omega \text{ (max) @ } V_{GS} = 10 \text{ V}$$



Device	Package	Marking	Remark
TMD5N40ZG/TMU5N40ZG	D-PAK/I-PAK	TMD5N40ZG/TMU5N40ZG	Halogen Free

Absolute Maximum Ratings

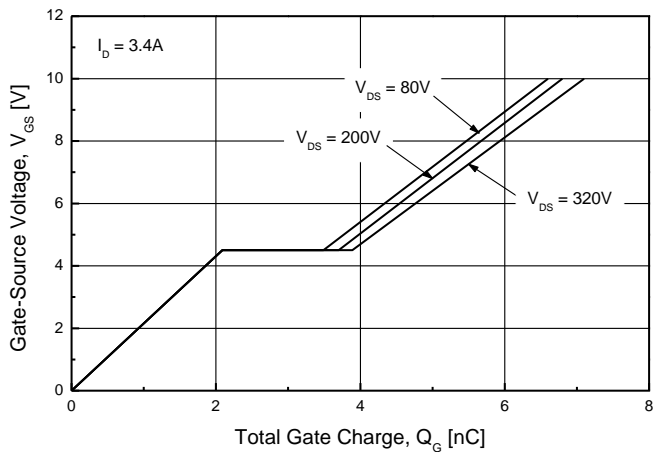
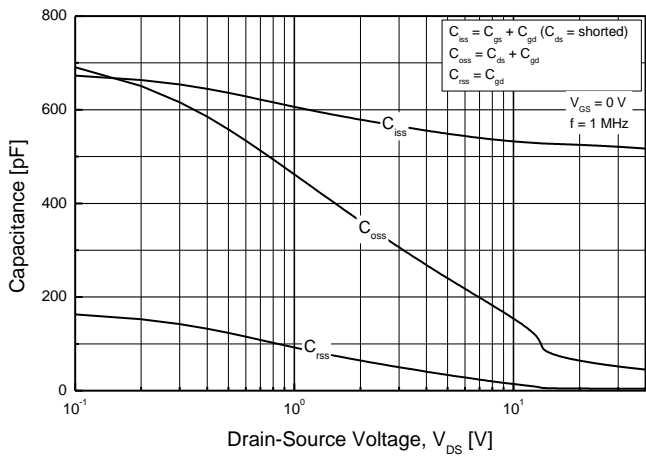
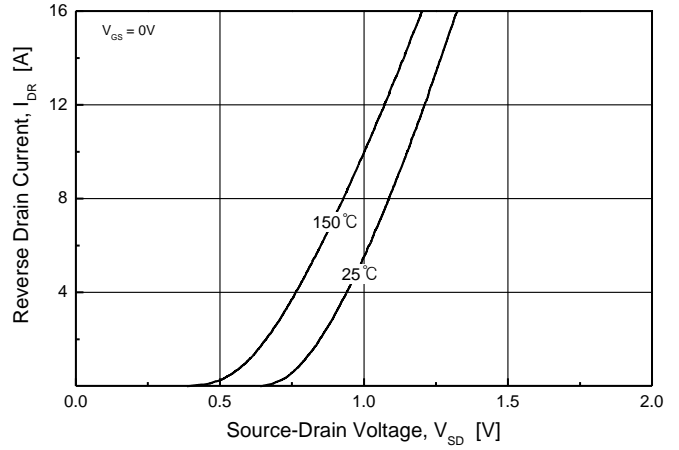
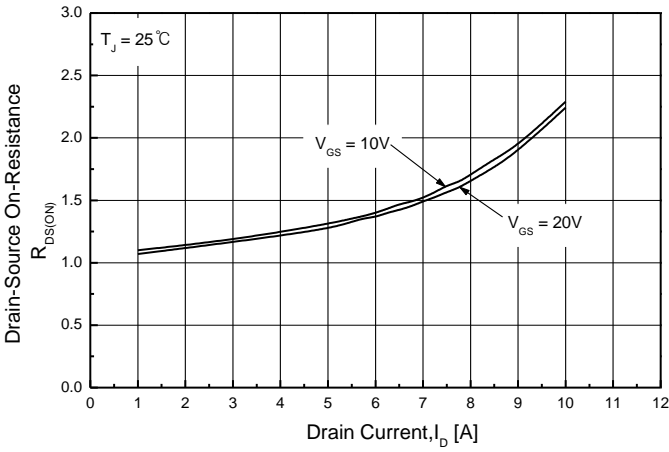
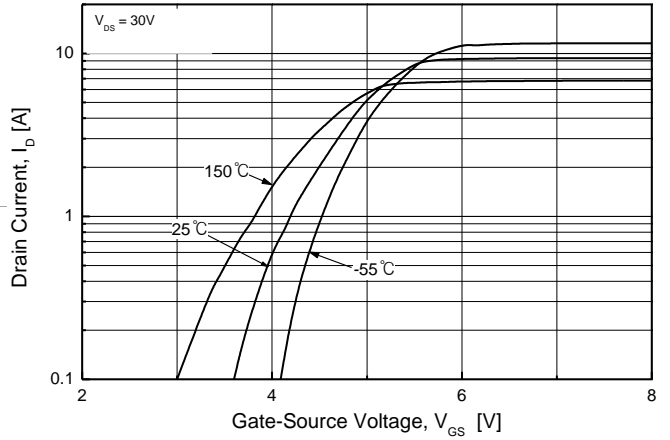
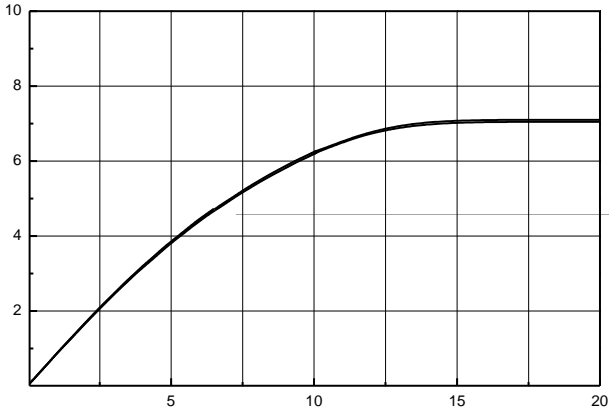
Parameter	Symbol	TMD5N40ZG/TMU5N40ZG	Unit
Drain-Source Voltage	V_{DS}	400	V
Gate-Source Voltage	V_{GS}	± 30	V
Continuous Drain Current	I_D	$T_C = 25 \text{ }^\circ\text{C}$	3.4*
		$T_C = 100 \text{ }^\circ\text{C}$	2.15*
Pulsed Drain Current (Note 1)	I_{DM}	13.6*	A
Single Pulse Avalanche Energy (Note 2)	E_{AS}	165	mJ
Repetitive Avalanche Current (Note 1)	I_{AR}	3.4	A
Repetitive Avalanche Energy (Note 1)	E_{AR}	5.0	mJ
Power Dissipation	P_D	$T_C = 25 \text{ }^\circ\text{C}$	50
		Derate above $25 \text{ }^\circ\text{C}$	0.4
Peak Diode Recovery dv/dt (Note 3)	dv/dt	4.5	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55~150	$^\circ\text{C}$
Maximum lead temperature for soldering purposes,	T_L	300	$^\circ\text{C}$

* Limited only by maximum junction temperature

Thermal Characteristics

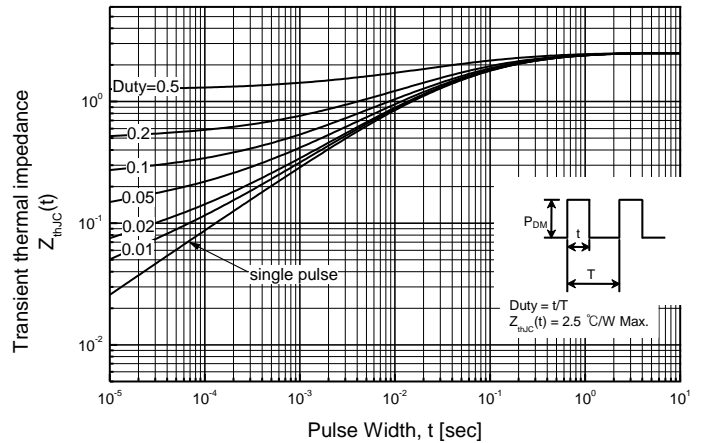
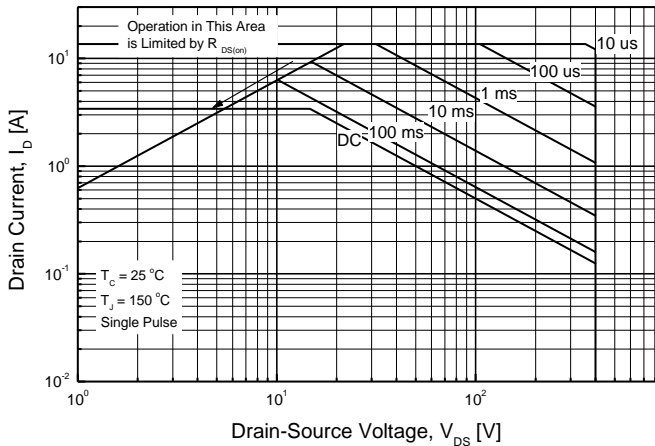
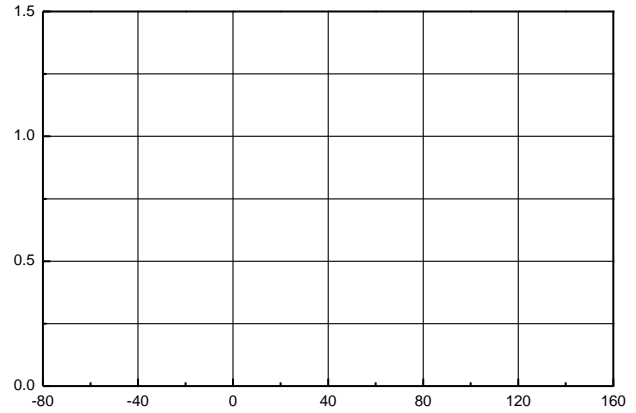
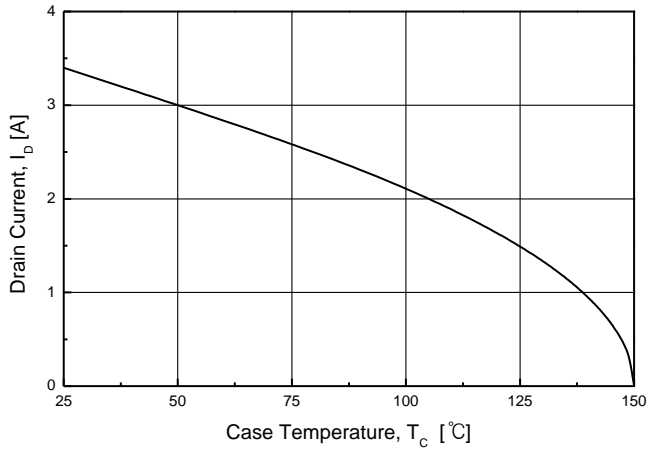
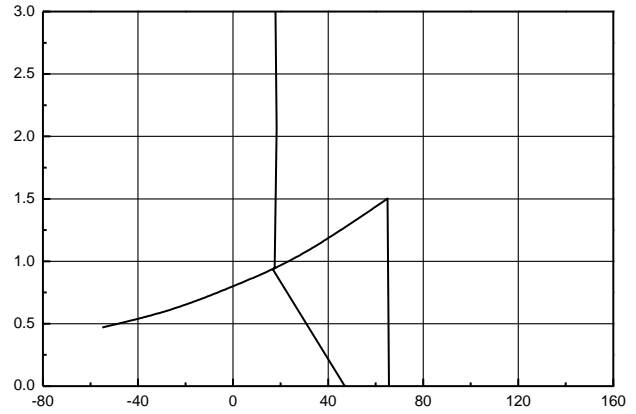
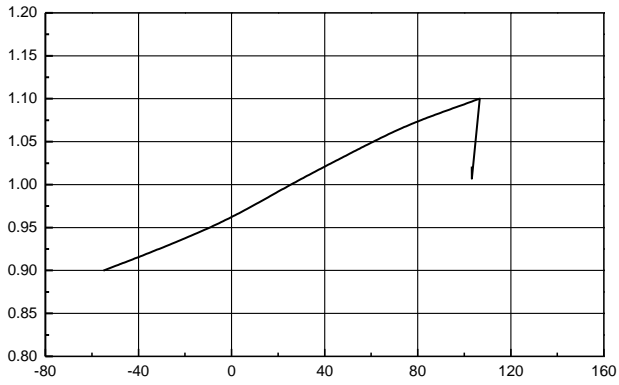
Parameter	Symbol	TMD5N40ZG/TMU5N40ZG	Unit
Maximum Thermal resistance, Junction-to-Case	$R_{\theta JC}$	2.5	$^\circ\text{C/W}$
Maximum Thermal resistance, Junction-to-Ambient	$R_{\theta JA}$	110	$^\circ\text{C/W}$

Parameter	Symbol	Test condition	Min	Typ	Max	Units
OFF						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	400	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	μA
		$V_{DS} = 320\text{ V}, T_C = 125^\circ\text{C}$	--	--	10	μA
Forward Gate-Source Leakage Current	I_{GSSF}	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	μA
Reverse Gate-Source Leakage Current	I_{GSSR}	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	μA
ON						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2	--	4	V
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 1.7\text{ A}$	--	1.2	1.6	Ω
Forward Transconductance ^(Note 4)	g_{FS}	$V_{DS} = 30\text{ V}, I_D = 1.7\text{ A}$	--	7	--	S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$	--	522	522	pF
Output Capacitance						

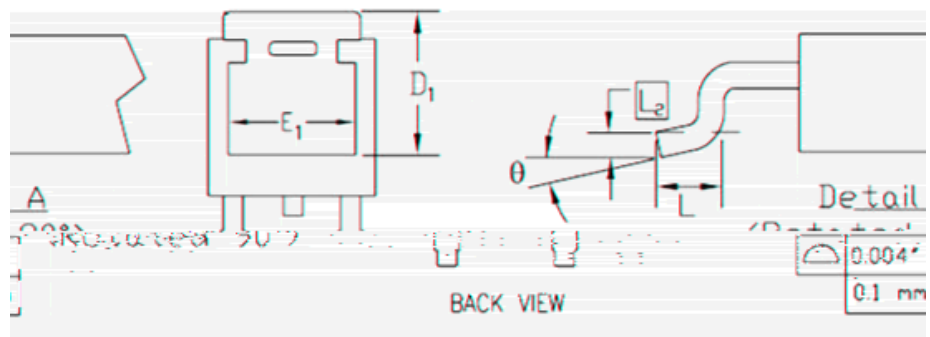
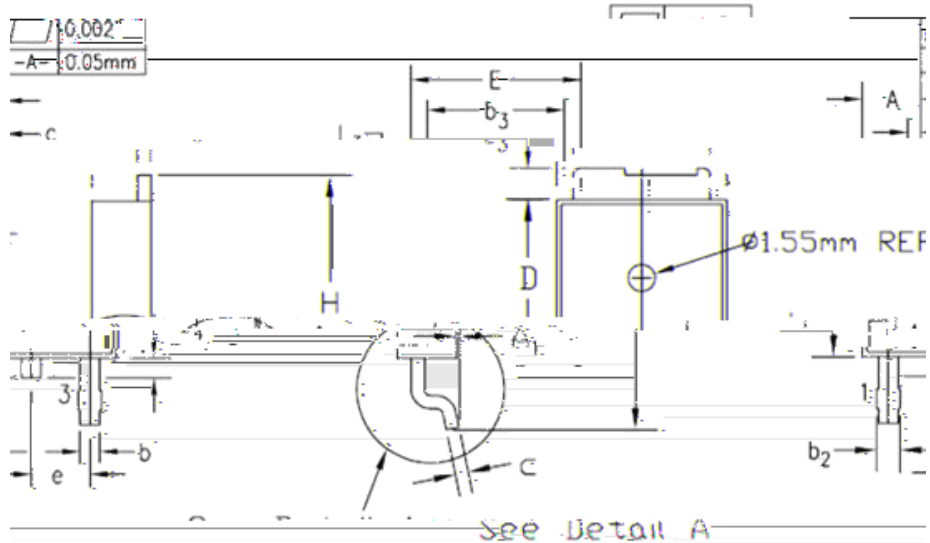




TMD5N40ZG/TMU5N40ZG

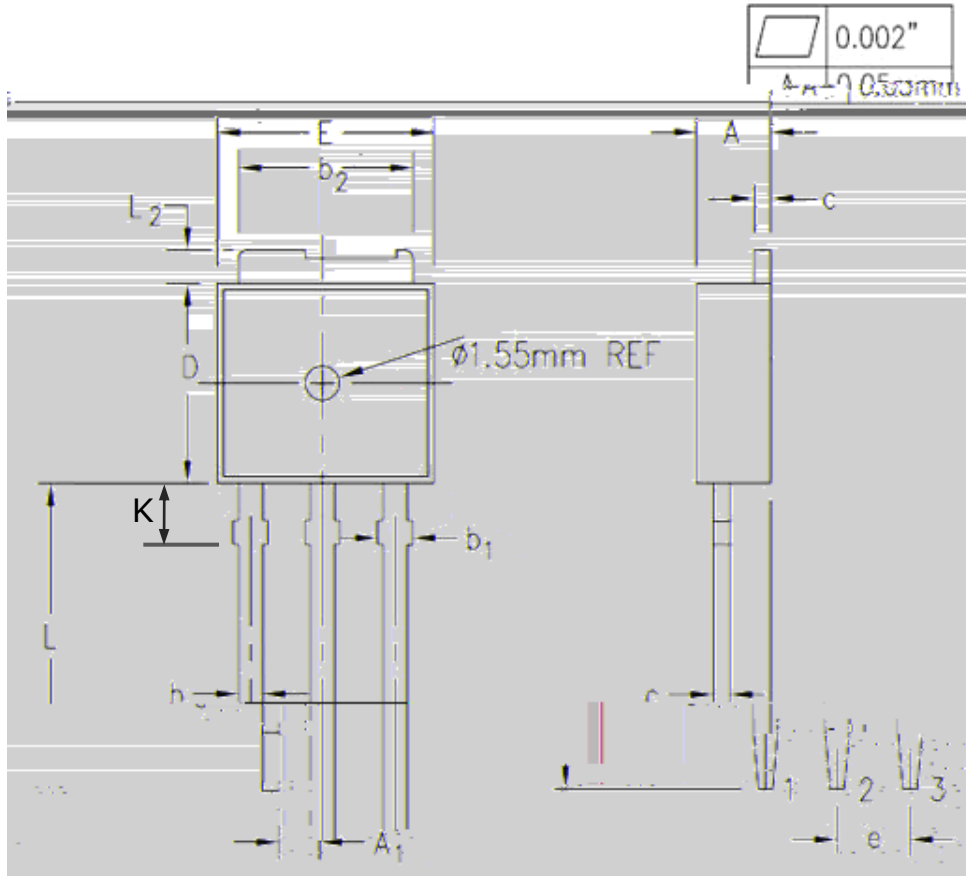


TO-252 (D-PAK) MECHANICAL DATA



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.385	0.398	9.79	10.13	
A1		0.005		0.13	
b	0.025	0.035	0.64	0.89	
b2	0.033	0.045	0.84	1.14	
b3	0.020	0.022	0.51	0.56	
D	0.235	0.245	5.97	6.22	
D1	0.205		5.21		2
E	0.250	0.265	6.35	6.73	
E1	0.190		4.83		2
e	0.090	BSC	2.29	BSC	
E2	0.380	0.410	9.65	10.41	
L	0.055	0.070	1.40	1.78	4
L2	0.020	BSC	0.51	BSC	
L3	0.035	0.050	0.89	1.27	
L4	0.025	0.040	0.64	1.01	3

TO-251 (I-PAK) MECHANICAL DATA



SYMBOL	INCHES		MILIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.086	0.094	2.19	2.39	
A1	0.040	0.045	1.02	1.14	
b	0.025	0.035	0.64	0.89	
b1	0.037	0.045	0.95	1.14	
b2	0.205	0.215	5.21	5.46	
c	0.018	0.023	0.46	0.58	
D	0.235	0.245	5.97	6.22	
E	0.250	0.265	6.35	6.73	
e	0.090 TYP.		2.28 TYP.		
L	0.350	0.380	8.89	9.65	
L2	0.035	0.050	0.89	1.27	
K	0.079	0.096	2.00	2.44	