



General Description

FSMOS[®]

$R_{DS(ON)}$, low gate charge, fast switching and excellent avalanche characteristics. The low V_{th} series is specially designed to use in synchronous rectification power systems with low driving voltage.

low

Features

- Low $R_{DS(ON)}$ & FOM
- Extremely low switching loss
- Excellent reliability and uniformity
- Fast switching and soft recovery



Applications

- PD charger
- Motor driver
- Switching voltage regulator
- DC-DC convertor
- Switched mode power supply

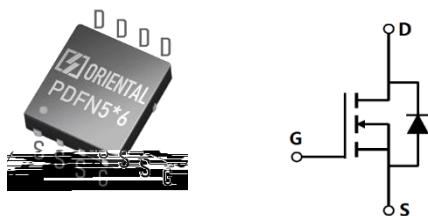
Key Performance Parameters

Parameter	Value	Unit
$V_{DS, min} @ T_{j(max)}$	60	V
$I_D, pulse$	210	A
$R_{DS(ON) max} @ V_{GS}=10V$	6	
Q_g	30	nC

Marking Information

Product Name	Package	Marking
SFS06R06GF	PDFN5*6	SFS06R06G

Package & Pin information



Absolute Maximum Ratings at $T_j=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Value	Unit
Drain source voltage	V_{DS}	60	V
Gate source voltage	V_{GS}	± 20	V
Continuous drain current ¹⁾ , $T_C=25^\circ\text{C}$	I_D	70	A
Pulsed drain current ²⁾ , $T_C=25^\circ\text{C}$	$I_{D,\text{pulse}}$	210	A
Continuous diode forward current ¹⁾ , $T_C=25^\circ\text{C}$	I_S	70	A
Diode pulsed current ²⁾ , $T_C=25^\circ\text{C}$	$I_{S,\text{Pulse}}$	210	A
Power dissipation ³⁾ , $T_C=25^\circ\text{C}$	P_D	87	W
Single pulsed avalanche energy ⁵⁾	E_{AS}	66	mJ
Operation and storage temperature	$T_{\text{stg}} \quad T_j$	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal resistance, junction-case	R	1.44	$^\circ\text{C}/\text{W}$
Thermal resistance, junction-ambient ⁴⁾	R	62	$^\circ\text{C}/\text{W}$

Electrical Characteristics at $T_j=25^\circ\text{C}$ unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Drain-source breakdown voltage	BV_{DSS}	60			V	$V_{GS}=0 \text{ V}, I_D=250 \text{ A}$
Gate threshold voltage	$V_{GS(\text{th})}$	1.0		2.5	V	$V_{DS}=V_{GS}, I_D=250 \text{ A}$
Drain-source on-state resistance	$R_{DS(\text{ON})}$		4.7	6		$V_{GS}=10 \text{ V}, I_D=20 \text{ A}$
Drain-source on-state resistance	$R_{DS(\text{ON})}$		6.4	10		$V_{GS}=4.5 \text{ V}, I_D=10 \text{ A}$
Gate-source leakage current	I_{GSS}			100	nA	$V_{GS}=20 \text{ V}$
				-100		$V_{GS}=-20 \text{ V}$
Drain-source leakage current	I_{DSS}			1	A	$V_{DS}=60 \text{ V}, V_{GS}=0 \text{ V}$
Gate resistance	R_G		2.8			



Dynamic Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Input capacitance	C _{iss}		2136		pF	V _{GS} =0 V, V _{DS} =50 V, kHz
Output capacitance	C _{oss}		332		pF	
Reverse transfer capacitance	C _{rss}		10.6		pF	
Turn-on delay time	t _{d(on)}		22.9		ns	V _{GS} =10 V, V _{DS} =50 V, R _G I _D =25 A
Rise time	t _r		6.5		ns	
Turn-off delay time	t _{d(off)}		45.7		ns	
Fall time	t _f		20.4		ns	

Gate Charge Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Total gate charge	Q _g		30		nC	V _{GS} =10 V, V _{DS} =50 V, I _D =25 A
Gate-source charge	Q _{gs}		5.8		nC	

Gate-

Electrical Characteristics Diagrams

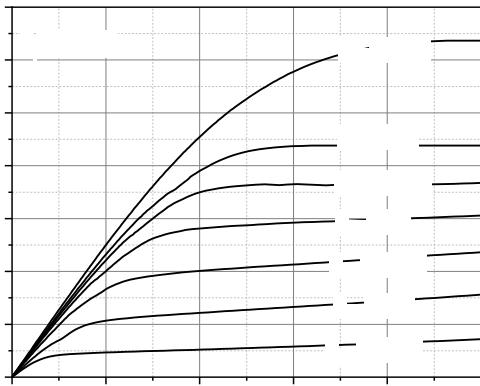


Figure 1. Typ. output characteristics

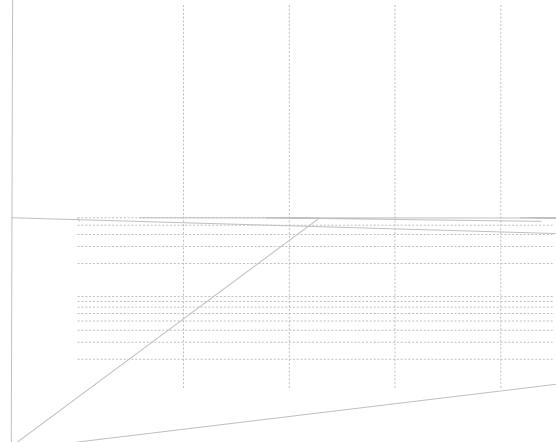


Figure 2. Typ. transfer characteristics

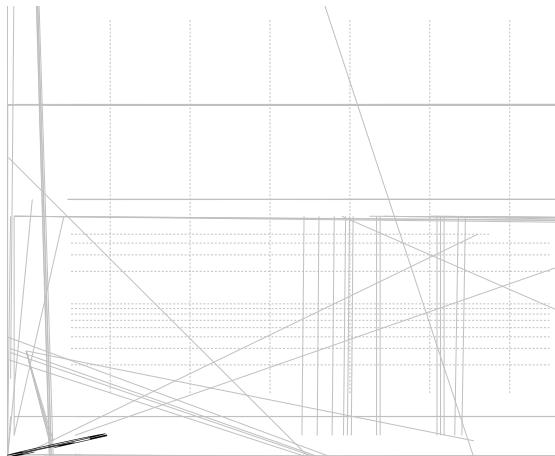


Figure 3. Typ. capacitances

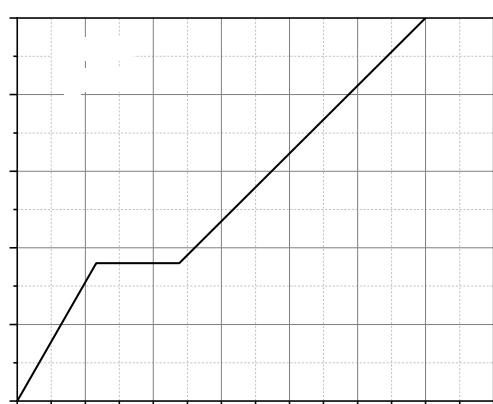


Figure 4. Typ. gate charge

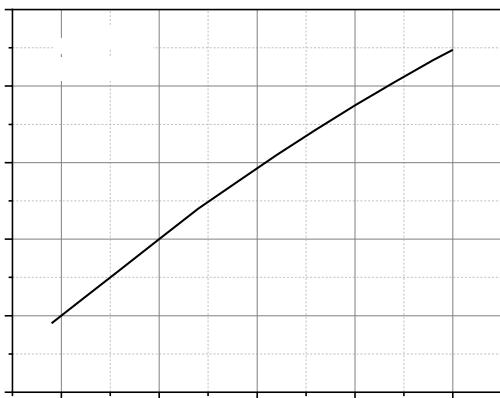


Figure 5. Drain-source breakdown voltage

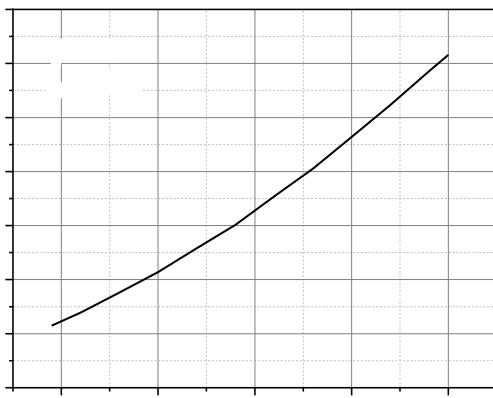
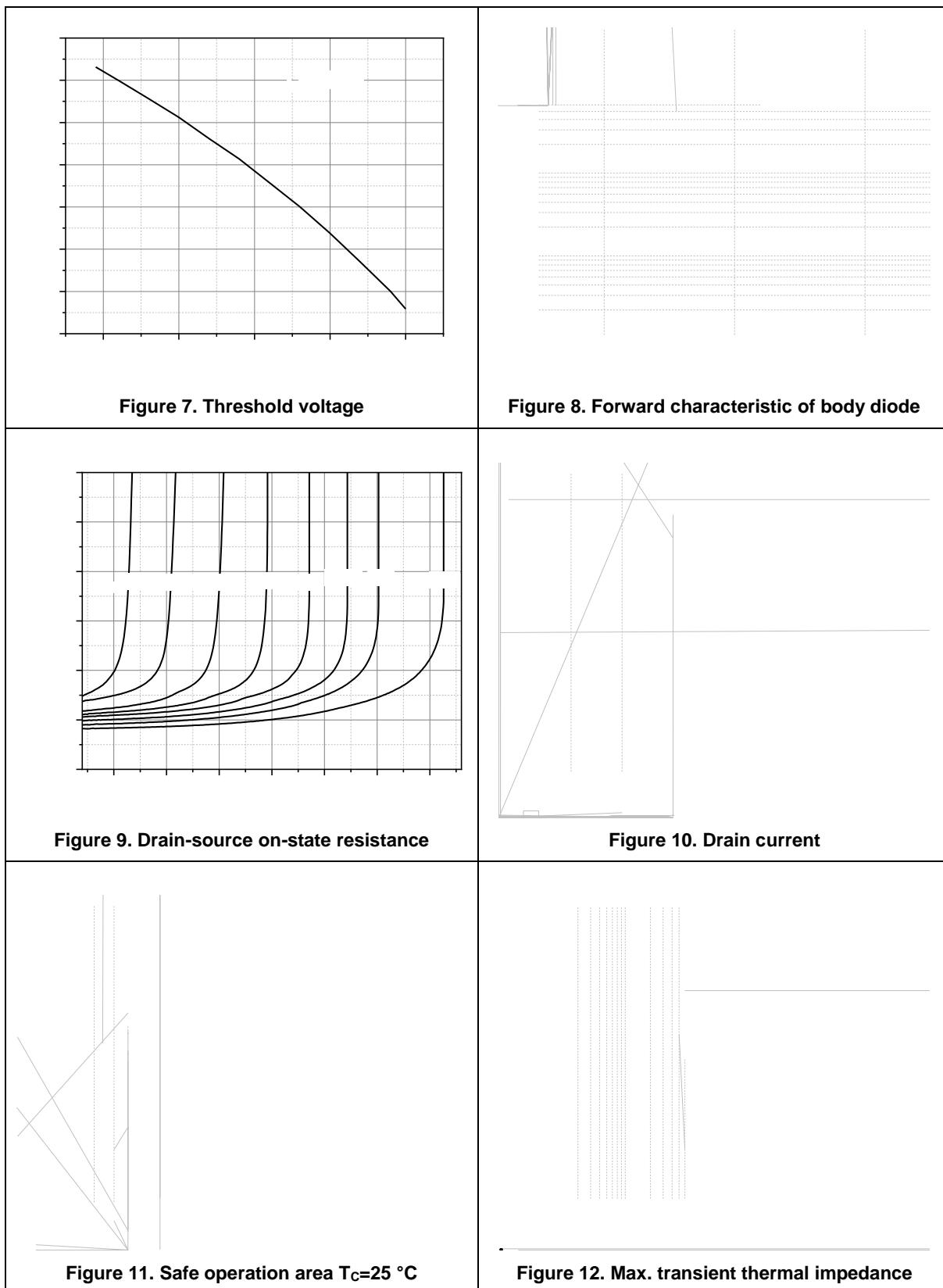


Figure 6. Drain-source on-state resistance



Test circuits and waveforms

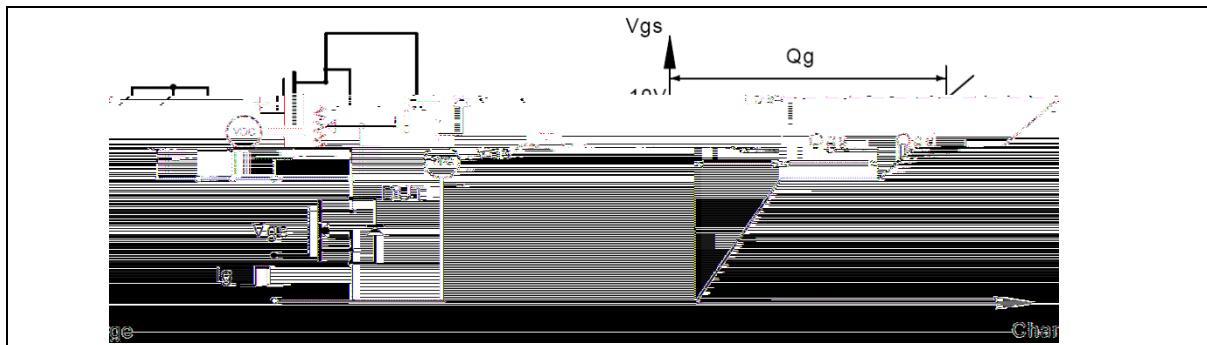


Figure 1. Gate charge test circuit & waveform

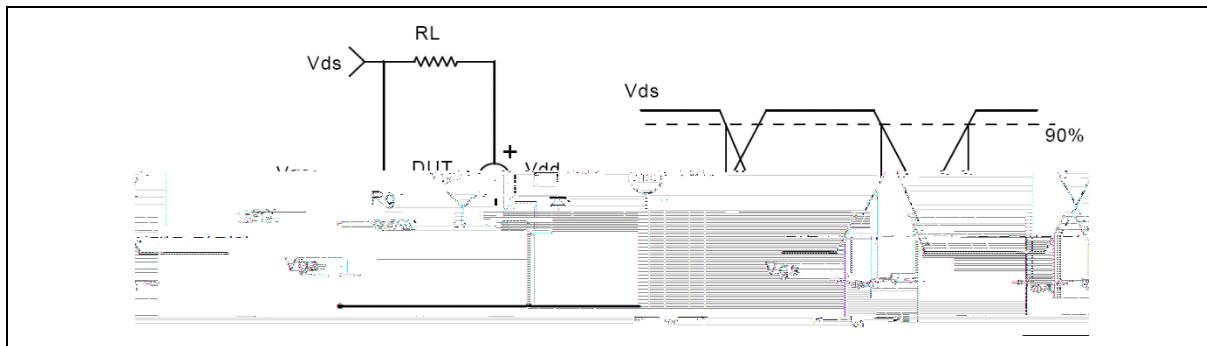


Figure 2. Switching time test circuit & waveforms

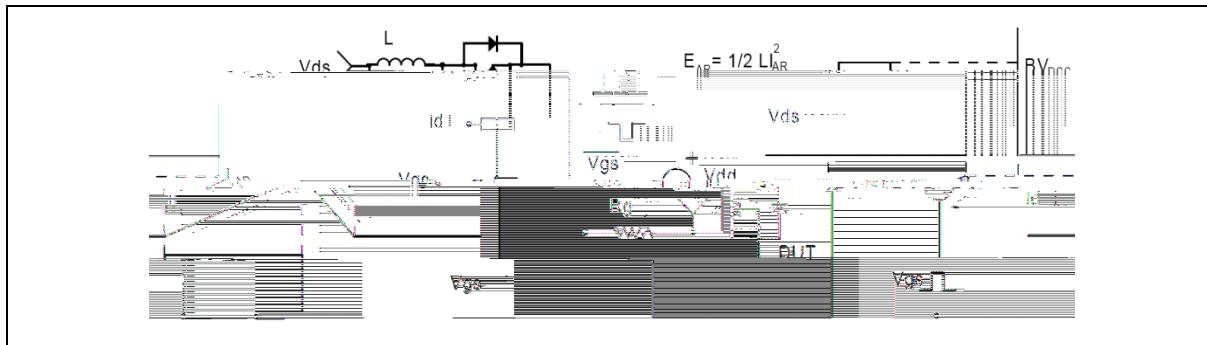


Figure 3. Unclamped inductive switching (UIS) test circuit & waveforms

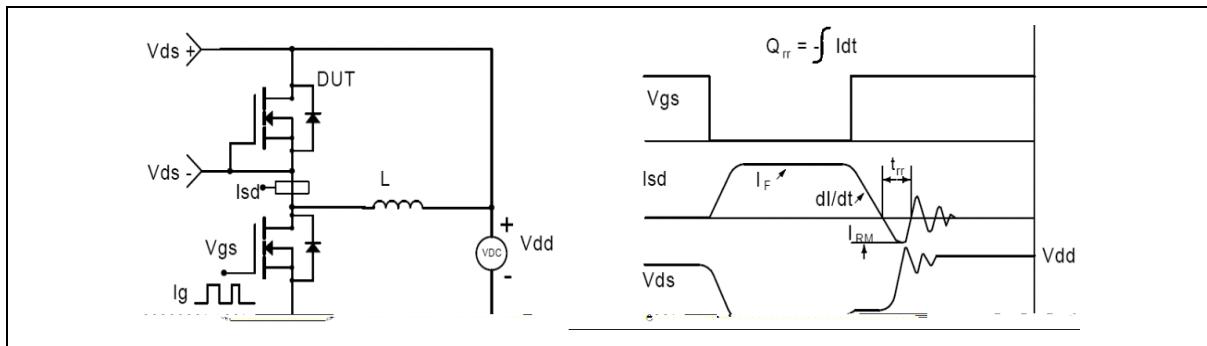
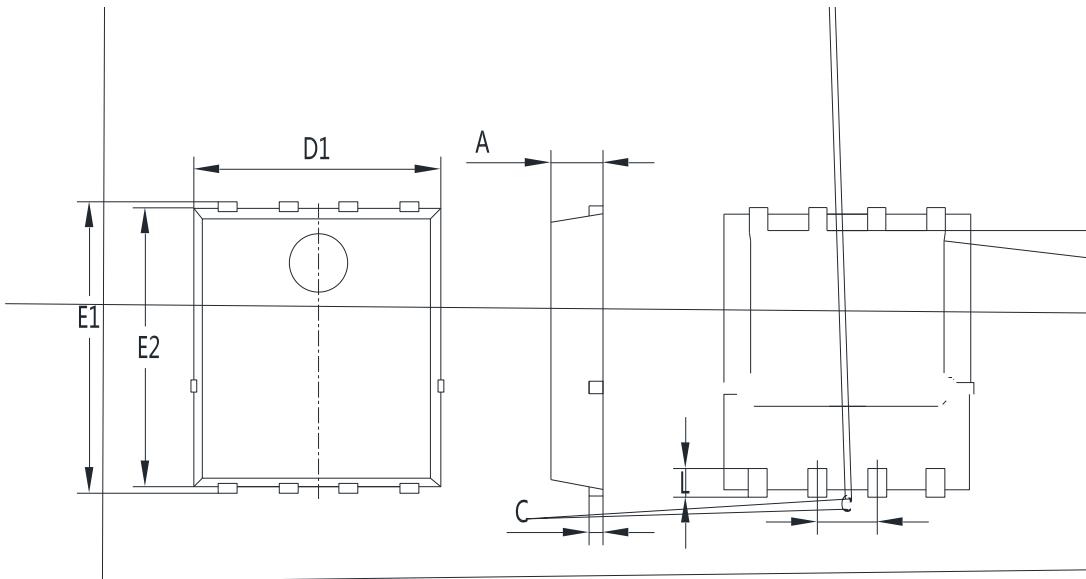


Figure 4. Diode reverse recovery test circuit & waveforms

Package Information



Symbol	mm		
	Min	Nom	Max
A	1.00	1.10	1.20
b	0.30	0.40	0.50
c	0.154	0.254	0.354
D1	5.00	5.20	5.40
D2	3.80	4.10	4.25
e	1.17	1.27	1.37
E1	5.95	6.15	6.35
E2	5.66	5.86	6.06
E4	3.52	3.72	3.92
H	0.40	0.50	0.60
L	0.30	0.60	0.70
L1	0.12 REF		
K	1.15	1.30	1.45

Version 1: PDFN5*6-P package outline dimension



Package Information

Symbol	Min	mm	Nom	Max
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SFS06R06G