

120V N-Ch Power MOSFET

Feature

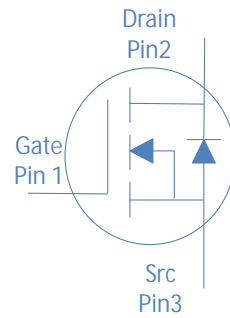
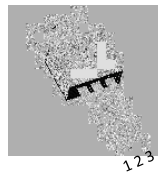
- High Speed Power Switching, Logic level
- Enhanced Body diode dv/dt capability
- Enhanced Avalanche Ruggedness
- 100% UIS Tested, 100% Rg Tested
- Lead Free

Application

- Synchronous Rectification in SMPS
- Hard Switching and High Speed Circuit
- Power Tools
- UPS
- Motor Control

V_{DS}		120	V
$R_{DS(on),typ}$	$V_{GS}=10V$	7.8	$m\Omega$
$R_{DS(on),typ}$	$V_{GS}=4.5V$	8.6	$m\Omega$
I_D (Silicon Limited)		109	A

TO-220



Part Number	Package	Marking
HGP100N12SL	TO-220	GP100N12SL

Absolute Maximum Ratings at $T_J=25$ (unless otherwise specified)

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current (Silicon Limited)	I_D	$T_C=25$	109	A
		$T_C=100$	77	
Drain to Source Voltage	V_{DS}	-	120	V
Gate to Source Voltage	V_{GS}	-	± 20	V
Pulsed Drain Current	I_{DM}	-	300	A
Avalanche Energy, Single Pulse	E_{AS}	$L=0.4mH, T_C=25$	320	mJ
Power Dissipation	P_D	$T_C=25$	125	W
Operating and Storage Temperature	T_J, T_{stg}	-	-55 to 175	

Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Case	$R_{\theta JC}$	0.7	$^{\circ}W$
Thermal Resistance Junction-Ambient	$R_{\theta JA}$	50	$^{\circ}W$

Electrical Characteristics at $T_j=25$ (unless otherwise specified)

Static Characteristics

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	120	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu A$	1.4	1.7	2.4	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS}=0V, V_{DS}=120V, T_j=25$	-	-	1	μA
		$V_{GS}=0V, V_{DS}=120V, T_j=100$	-	-	100	μA
Gate to Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
Drain to Source on Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=20A$	-	7.8	10	m Ω
		$V_{GS}=4.5V, I_D=20A$	-	8.6	13.5	m Ω
Transconductance	g_{fs}	$V_{DS}=5V, I_D=20A$	-	70	-	S
		$V_{GS}=0V, V_{DS}$ Open, $f=1MHz$	-	2.5	-	Ω

Dynamic Characteristics

Input Capacitance	C_{iss}		-	4730	-	
Output Capacitance	C_{oss}	$V_{GS}=0V, V_{DS}=60V, f=1MHz$	-	242	-	pF
Reverse Transfer Capacitance	C_{rss}		-	11	-	
Total Gate Charge	$Q_g(10V)$		-	66	-	
Total Gate Charge	$Q_g(4.5V)$		-	32	-	
Gate to Source Charge	Q_{gs}	$V_{DD}=60V, I_D=20A, V_{GS}=10V$	-	14	-	nC
Gate to Drain (Miller) Charge	Q_{gd}		-	6	-	
			-	18	-	
Rise time	t_r	$V_{DD}=60V, I_D=20A, V_{GS}=10V,$	-	21	-	ns
Turn off Delay Time		$R_G=10\Omega,$		39	-	
				19	-	

Reverse Diode Characteristics

Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_F=20A$	-			
Reverse Recovery Time			-	60	-	ns
Reverse Recovery Charge	Q_{rr}		-		-	nC

Fig 1. Typical Output Characteristics

Figure 3. On-Resistance vs. Drain Current and Gate Voltage

Figure 4. Normalized On-Resistance vs. Junction Temperature

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

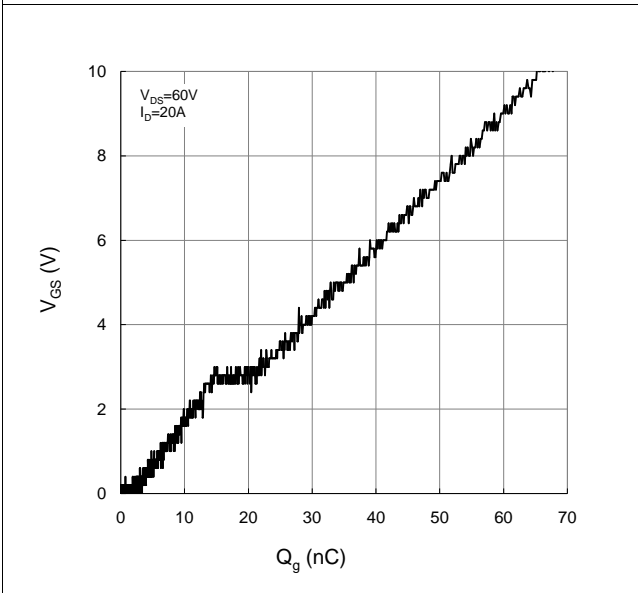


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

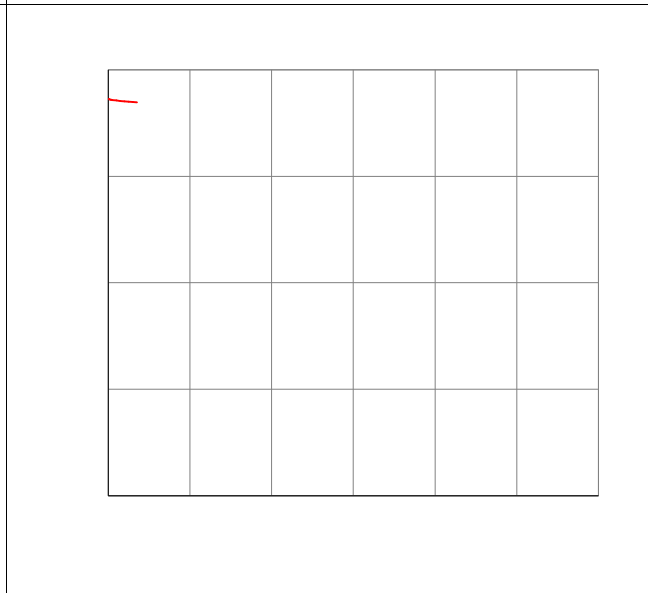


Figure 9. Maximum Safe Operating Area

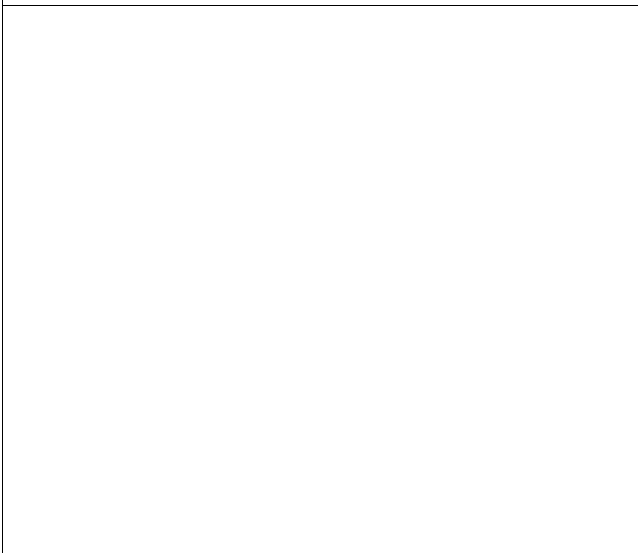


Figure 10. Maximum Drain Current vs. Case Temperature

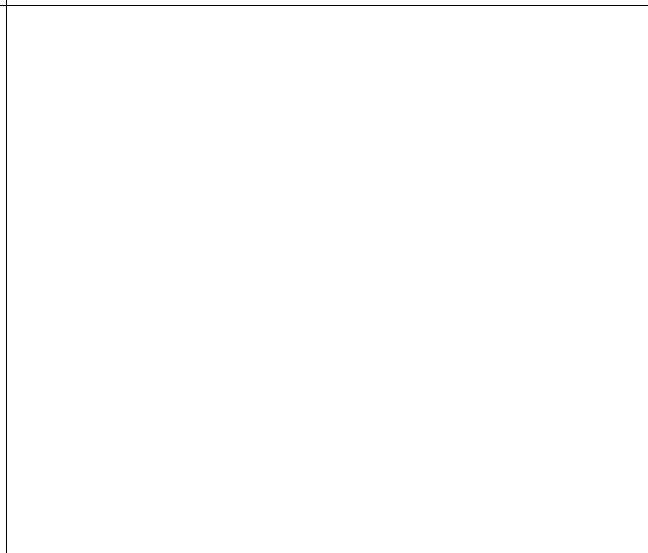
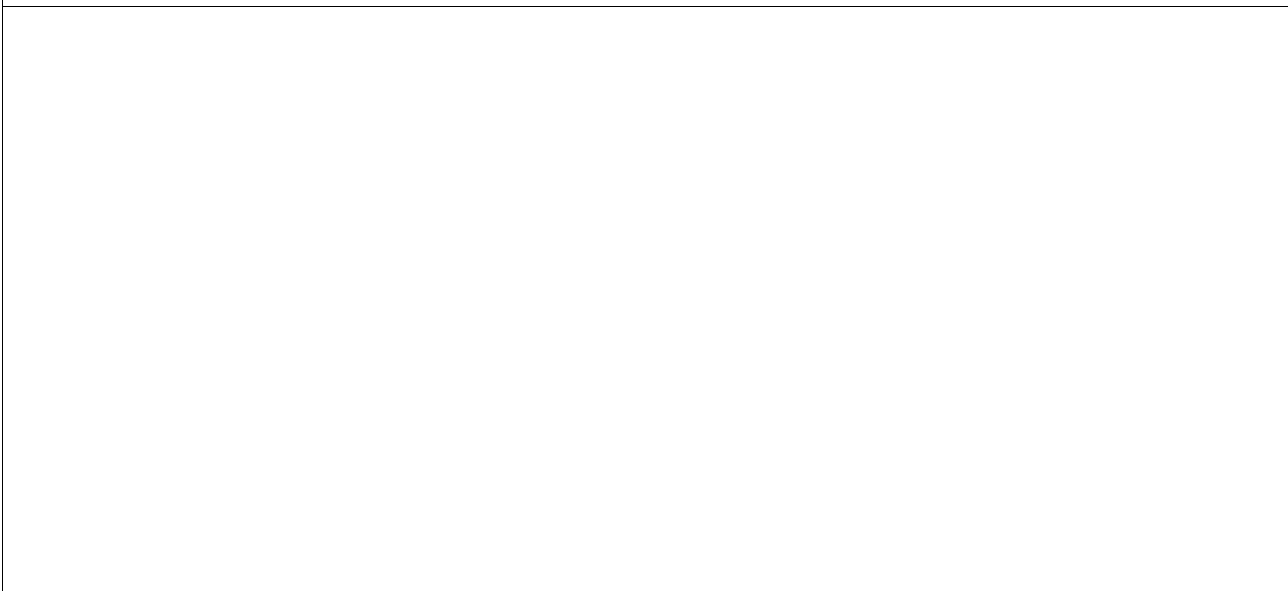


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Case



Inductive switching Test

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Gate Charge Test

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Uclamped Inductive Switching (UIS) Test

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Diode Recovery Test

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