150V N-Ch Power MOSFET

V_{DS}		150	V
$R_{DS(on),typ}$	V_{GS}=10V	65	mΩ
I_D		18	A

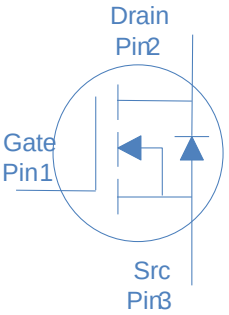
Feature

- High Speed Power Switching
- Enhanced Body diode dv/dt capability
- Enhanced Avalanche Ruggedness
- 100% UIS Tested, 100% Rg Tested
- Lead Free

Application

- Synchronous Rectification in SMPS
- Hard Switching and High Speed Circuit
- Power Tools
- UPS
- Motor Control

TO-252



Part Number	Package	Marking
HGD750N15M	TO-252	GD750N15M

Absolute Maximum Ratings at T_j=25 (unless otherwise specified)

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current (Silicon Limited)	I_D	T_C=25	18	A
		T_C=100	13	
Drain to Source Voltage	V_{DS}	-	150	V
Gate to Source Voltage	V_{GS}	-	±20	V
Pulsed Drain Current	I_{DM}	-	40	A
Avalanche Energy, Single Pulse	E_{AS}	L=0.3mH, T_C=25	3.75	mJ
Power Dissipation	P_D	T_C=25	60	W
Operating and Storage Temperature	T_J, T_{stg}	-	-55 to175	

Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Case	$R_{\theta JC}$	2.5	/W
Thermal Resistance Junction-Ambient	$R_{\theta JA}$	60	/W

Electrical Characteristics at T_j=25 (unless otherwise specified)

Static Characteristics

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=250μA	150	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=250μA	2	3.2	4	
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS}=0V, V_{DS}=150V, T_j=25	-	-	1	μA
		V_{GS}=0V, V_{DS}=150V, T_j=100	-	-	100	
Gate to Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Drain to Source on Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=10A	-	65	75	mΩ
Transconductance	g_{fs}	V_{DS}=5V, I_D=10A	-	12	-	S
Gate Resistance	R_G	V_{GS}=0V, V_{DS} Open, f=1MHz	-	5.0	-	Ω

Dynamic Characteristics

Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=75V, f=1MHz	-	616	-	pF
Output Capacitance	C_{oss}		-	35	-	
Reverse Transfer Capacitance	C_{rss}		-	13	-	
Total Gate Charge	Q_g	V_{DD}=75V, I_D=10A, V_{GS}=10V	-	11	-	nC
Gate to Source Charge	Q_{gs}		-	2.4	-	
Gate to Drain (Miller) Charge	Q_{gd}		-	4	-	
Turn on Delay Time	$t_{d(on)}$	V_{DD}=75V, I_D=10A, V_{GS}=10V, R_G=10Ω,	-	12	-	ns
Rise time	t_r		-	8	-	
Turn off Delay Time	$t_{d(off)}$		-	14	-	
Fall Time	t_f		-	3	-	

Reverse Diode Characteristics

Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_F=10A	-	0.9	1.2	V
Reverse Recovery Time	t_{rr}	V_R=75V, I_F=10A, dI_F/dt=100A/μs	-	60	-	ns
Reverse Recovery Charge	Q_{rr}		-	168	-	nC

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

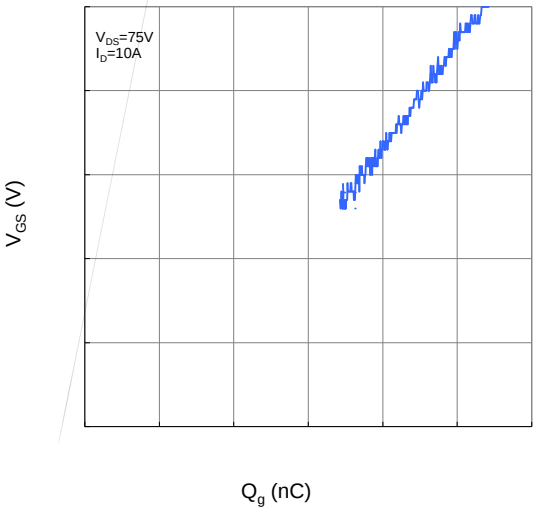


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

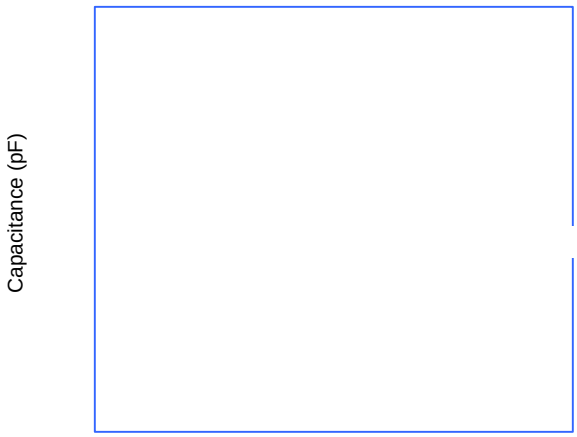


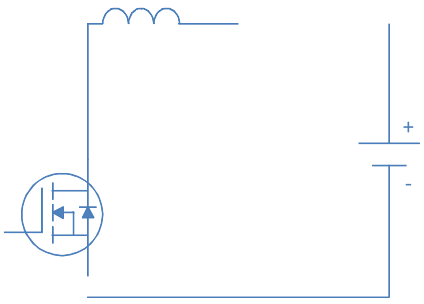
Figure 9. Maximum Safe Operating Area

Figure 10. Maximun Drain Current vs. Case Temperature

ınsient Thermal Impedance, Junction-to-Case

Inductive switching Test	

Gate Charge Test	

Uclamped Inductive Switching (UIS) Test	
	

Diode Recovery Test	

Package Outline

TO-252, 2 leads