

100V N-Ch Power MOSFET

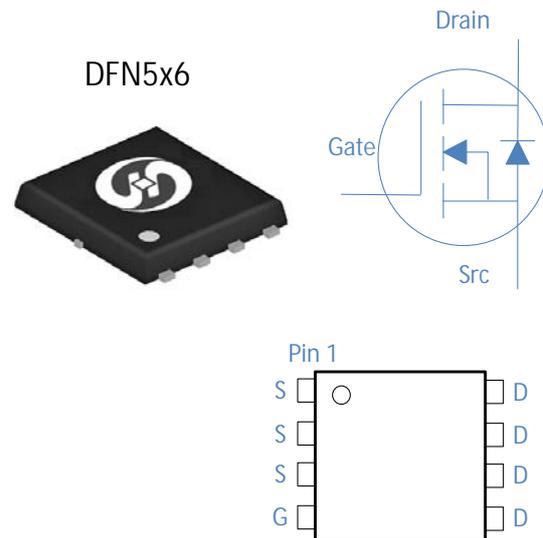
Feature

- Optimized for high speed smooth switching, Logic level
- Enhanced Body diode dv/dt capability
- Enhanced Avalanche Ruggedness
- 100% UIS Tested, 100% Rg Tested

Application

- DC-DC Conversion
- Hard Switching and High Speed Circuit
- Power Tools
- UPS
- SSR

V_{DS}		100	V
$R_{DS(on),typ}$	$V_{GS}=10V$	4.6	$m\Omega$
$R_{DS(on),typ}$	$V_{GS}=4.5V$	5.6	$m\Omega$
I_D (Silicon Limited)		115	A
I_D (Package Limited)		60	A



Part Number	Package	Marking
HGN052N10SL	DFN5x6	GN052N10SL

Absolute Maximum Ratings at $T_j=25$ (unless otherwise specified)

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current (Silicon Limited)	I_D	$T_C=25$	115	A
		$T_C=100$	73	
		Continuous Drain Current (Package Limited)	$T_C=25$	
Drain to Source Voltage	V_{DS}	-	100	V
Gate to Source Voltage	V_{GS}	-	± 20	V
Pulsed Drain Current	I_{DM}	-	300	A
Avalanche Energy, Single Pulse	E_{AS}	$L=0.3mH, T_C=25$	240	mJ
Power Dissipation	P_D	$T_C=25$	125	W
Operating and Storage Temperature	T_J, T_{stg}	-	-55 to 150	

Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Case	R_{JC}	1	W/W
Thermal Resistance Junction-Ambient	R_{JA}	50	W/W

Electrical Characteristics at $T_J=25$ (unless otherwise specified)
Static Characteristics

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	100	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu A$	1.4	1.7	2.4	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS}=0V, V_{DS}=100V, T_J=25$	-	-	1	μA
		$V_{GS}=0V, V_{DS}=100V, T_J=100$	-	-	100	
Gate to Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
Drain to Source on Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=20A$	-	4.6	5.2	$m\Omega$
		$V_{GS}=4.5V, I_D=20A$	-	5.6	7	$m\Omega$
Transconductance	g_{fs}	$V_{DS}=5V, I_D=20A$	-	70	-	S
Gate Resistance	R_G	$V_{GS}=0V, V_{DS}$ Open, $f=1MHz$	-	3.5	-	Ω

Dynamic Characteristics

Input Capacitance	C_{iss}	$V_{GS}=0V, V_{DS}=50V, f=1MHz$	-	4351	-	pF
Output Capacitance	C_{oss}		-	323	-	
Reverse Transfer Capacitance	C_{rss}		-	12	-	
Total Gate Charge	$Q_g(10V)$	$V_{DD}=50V, I_D=20A, V_{GS}=10V$	-	60	-	nC
Total Gate Charge	$Q_g(4.5V)$		-	26	-	
Gate to Source Charge	Q_{gs}		-	8	-	
Gate to Drain (Miller) Charge	Q_{gd}		-	10	-	
Turn on Delay Time	$t_{d(on)}$	$V_{DD}=50V, I_D=20A, V_{GS}=10V,$ $R_G=10\Omega,$	-	15	-	ns
Rise time	t_r		-	6	-	
Turn off Delay Time	$t_{d(off)}$		-	42	-	
Fall Time	t_f		-	8	-	

Reverse Diode Characteristics

Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_F=20A$	-	0.9	1.2	V
Reverse Recovery Time	t_{rr}	$V_R=50V, I_F=20A, di_F/dt=500A/\mu s$	-	50	-	ns
Reverse Recovery Charge	Q_{rr}		-	275	-	nC

Fig 1. Typical Output Characteristics

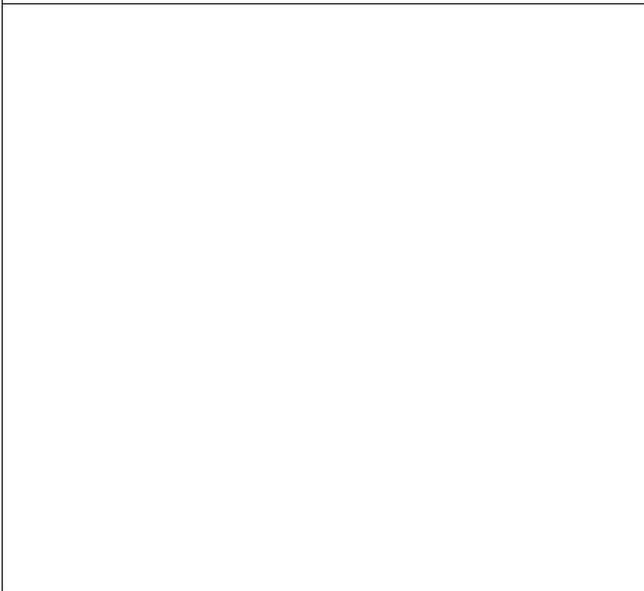


Figure 2. On-Resistance vs. Gate-Source Voltage

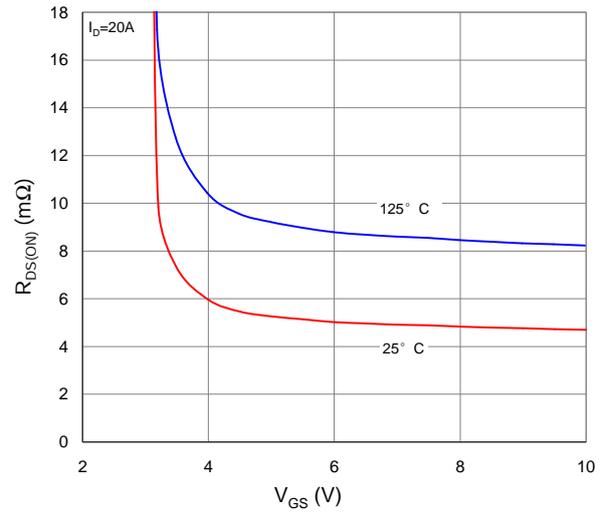


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

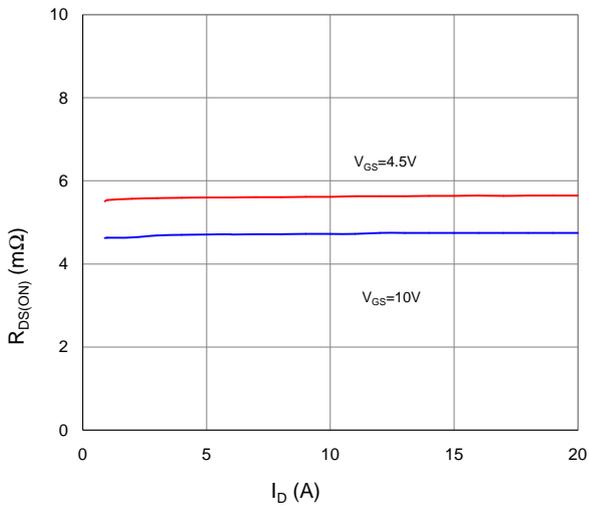


Figure 4. Normalized On-Resistance vs. Junction Temperature

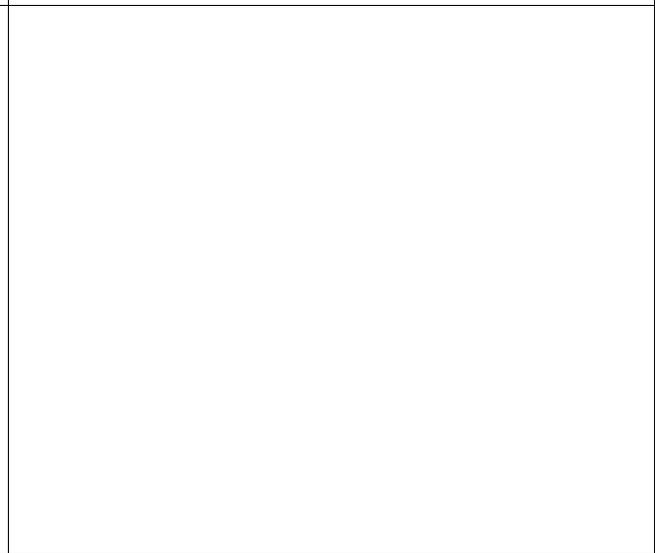


Figure 5. Typical Transfer Characteristics

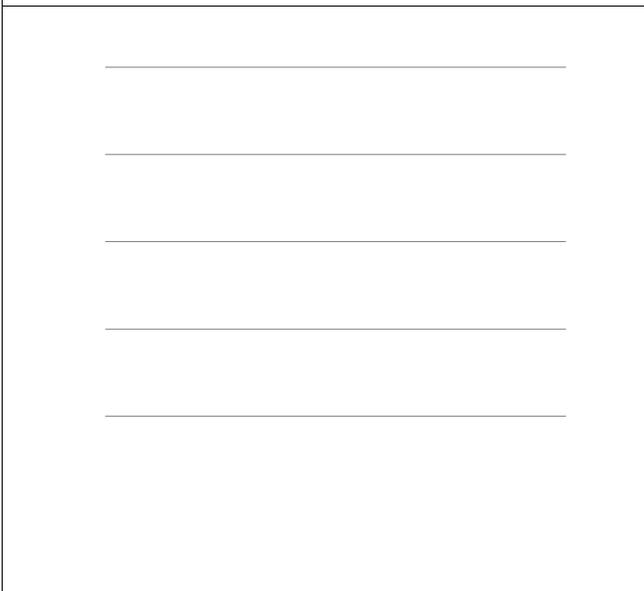


Figure 6. Typical Source-Drain Diode Forward Voltage

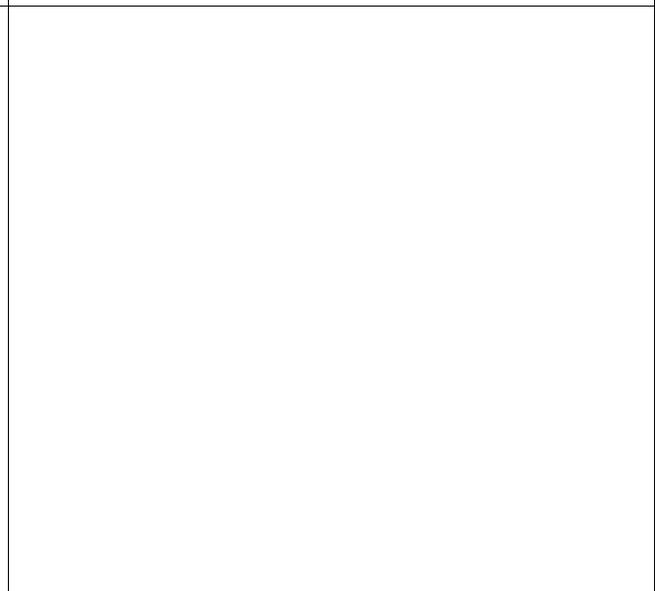


Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

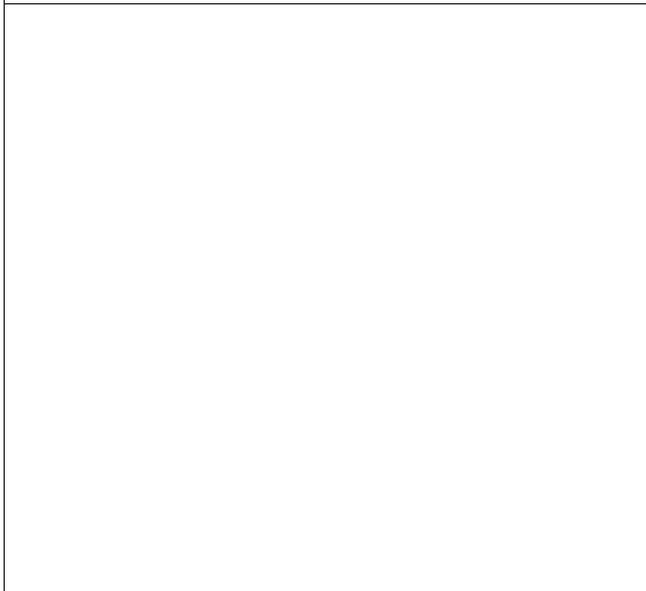


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

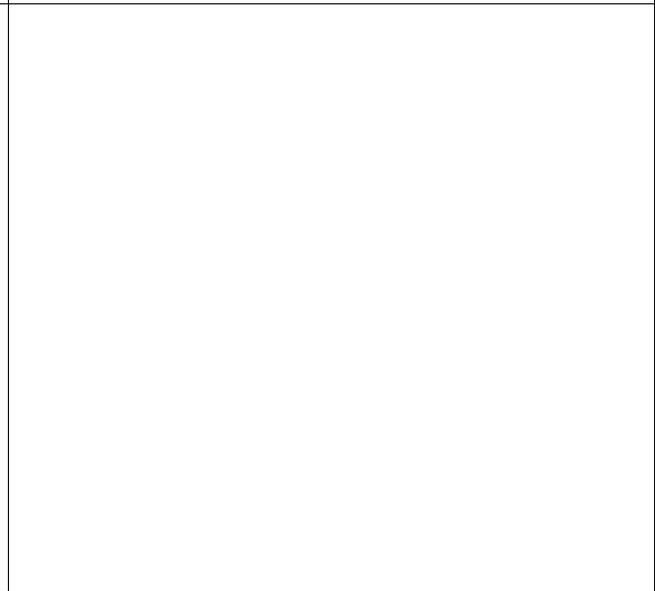


Figure 9. Maximum Safe Operating Area

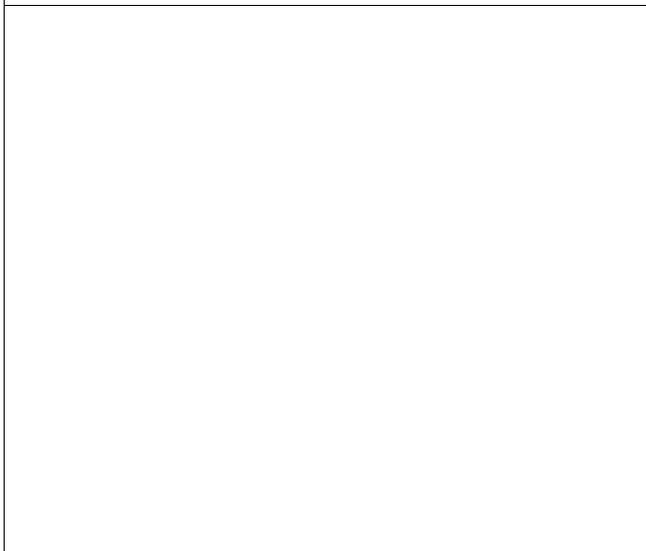


Figure 10. Maximun Drain Current vs. Case Temperature

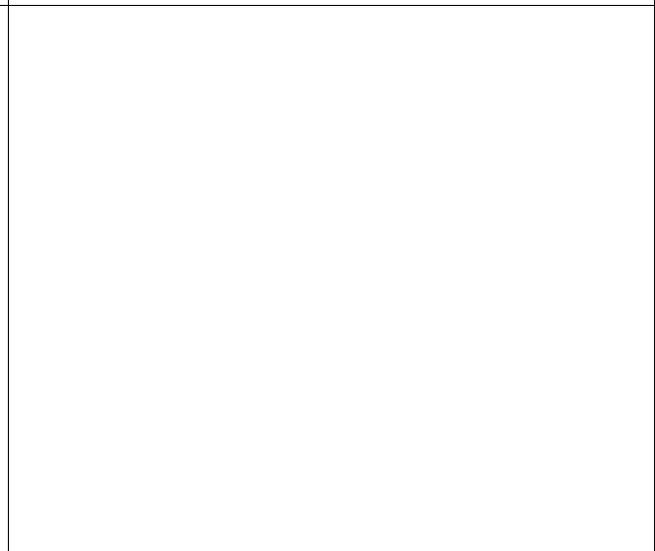
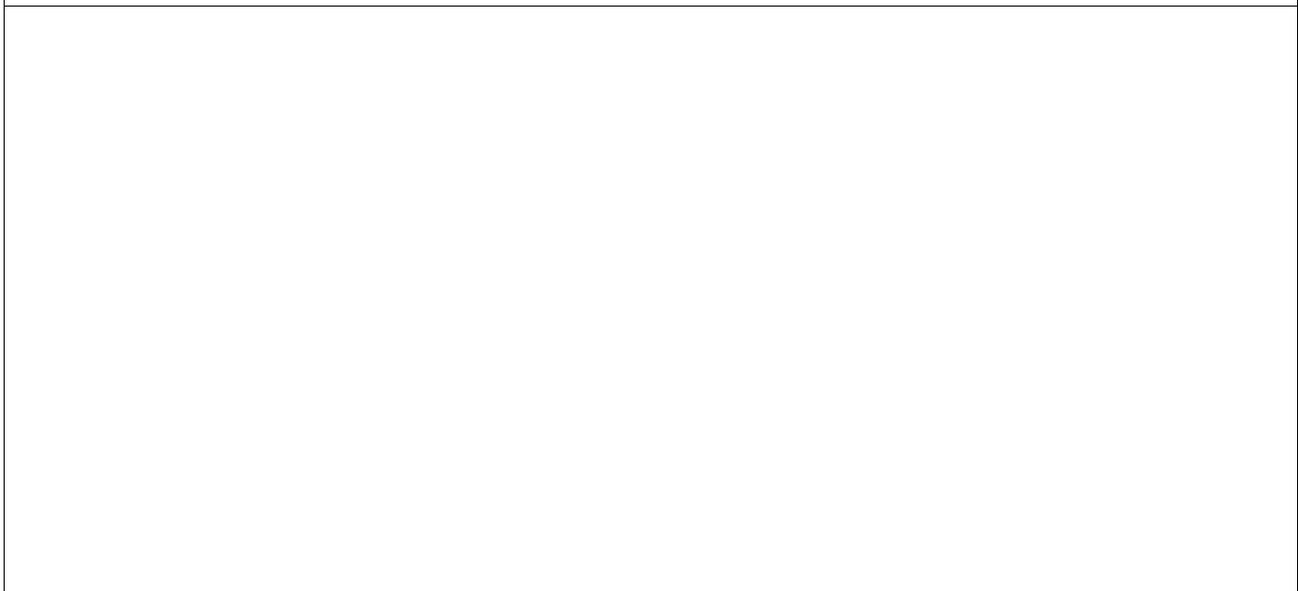


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Case



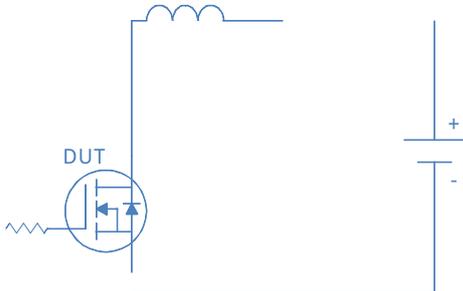
Inductive switching Test

--	--

Gate Charge Test

--	--

Uclamped Inductive Switching (UIS) Test

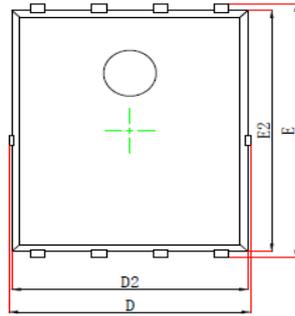
 <p>The diagram illustrates the UIS test setup. A MOSFET, labeled 'DUT', is connected in series with an inductor and a diode. The MOSFET's gate is driven by a pulse source (represented by a resistor and a pulse). The inductor is connected to the MOSFET's drain. The diode is connected in parallel with the MOSFET's drain, with its cathode to the MOSFET's drain and its anode to the MOSFET's source. The diode is represented by a vertical line with a horizontal bar at the top and a '-' sign at the bottom.</p>	
--	--

Diode Recovery Test

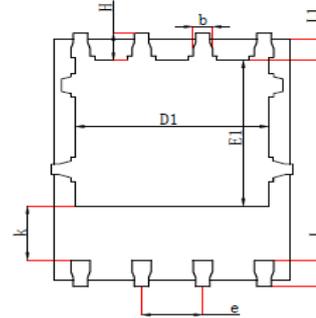
--	--

Package Outline

DFN5x6_P, 8 Leads



Top View
[顶视图]



Bottom View
[背视图]



Side View
[侧视图]

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A3	0.254 REF		0.010REF	
D	4.680	5.120	0.184	0.202
E	5.900	6.126	0.232	0.241
D1	3.610	4.110	0.142	0.162
E1	3.380	3.780	0.133	0.149
D2	4.800	5.000	0.189	0.197
E2	5.674	5.826	0.223	0.229
k	1.100	1.390	0.043	0.055
b	0.330	0.510	0.013	0.020
e	1.270TYP		1.270TYP	
L	0.510	0.711	0.020	0.028
L1	0.424	0.576	0.017	0.023
H	0.410	0.726	0.016	0.029
θ	0°	12°	0°	12°