150V N-Ch Power MOSFET

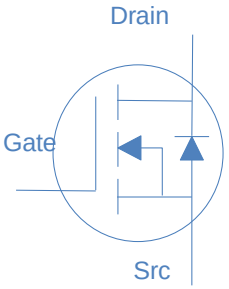
Feature

- High Speed Power Switching, Logic Level
- Enhanced Body diode dv/dt capability
- Enhanced Avalanche Ruggedness
- 100% UIS Tested, 100% Rg Tested
- Lead Free, Halogen Free

V_{DS}		150	V
$R_{DS(on),typ}$	V_{GS}=10V	8	mΩ
$R_{DS(on),typ}$	V_{GS}=4.5V	9.4	mΩ
$I_{D\ (Sillicon\ Limited)}$		73.9	A
$I_{D\ (Package\ Limited)}$		60	A

Application

- Synchronous Rectification in SMPS
- Hard Switching and High Speed Circuit
- DC/DC in Telecoms and Inductrial



Part Number	Package	Marking
HGN115N15SL	DFN5*6	GN115N15SL

Absolute Maximum Ratings at T_j=25 (unless otherwise specified)

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current (Silicon Limited)	I_D	T_C=25	74	A
		T_C=100	47	
Continuous Drain Current (Package Limited)		T_C=25	60	
Drain to Source Voltage	V_{DS}	-	150	V
Gate to Source Voltage	V_{GS}	-	±20	V
Pulsed Drain Current	I_{DM}	-	250	A
Avalanche Energy, Single Pulse	E_{AS}	L=0.4mH, T_C=25	125	mJ
Power Dissipation	P_D	T_C=25	114	W
Operating and Storage Temperature	T_J, T_{stg}	-	-55 to150	

Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Ambient	$R_{\theta JA}$	55	/W
Thermal Resistance Junction-Case	$R_{\theta JC}$	1.1	/W

Electrical Characteristics at T_j=25 (unless otherwise specified)

Static Characteristics

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=250μA	150	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=250μA	1	2	3	
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS}=0V, V_{DS}=150V, T_j=25	-	-	1	μA
		V_{GS}=0V, V_{DS}=150V, T_j=100	-	-	100	
Gate to Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Drain to Source on Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=20A	-	8	11.5	mΩ
		V_{GS}=4.5V, I_D=20A	-	9.4	15	
Transconductance	g_{fs}	V_{DS}=5V, I_D=20A	-	85	-	S
Gate Resistance	R_G	V_{GS}=0V, V_{DS} Open, f=1MHz	-	2.6	-	Ω

Dynamic Characteristics

Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=75V, f=1MHz	-	3784	-	pF
Output Capacitance	C_{oss}		-	257	-	
Reverse Transfer Capacitance	C_{rss}		-	7.3	-	
Total Gate Charge	Q_g(10V)	V_{DD}=75V, I_D=20A, V_{GS}=10V	-	48	-	nC
Total Gate Charge	Q_g(4.5V)		-	21	-	
Gate to Source Charge	Q_{gs}		-	11	-	
Gate to Drain (Miller) Charge	Q_{gd}		-	5	-	
Turn on Delay Time	$t_{d(on)}$	V_{DD}=75V, I_D=20A, V_{GS}=10V, R_G=10Ω,	-	18	-	ns
Rise time	t_r		-	8	-	
Turn off Delay Time	$t_{d(off)}$		-	29	-	
Fall Time	t_f		-	10	-	

Reverse Diode Characteristics

Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_F=20A	-	0.9	1.2	V
Reverse Recovery Time	t_{rr}	V_R=75V, I_F=20A, dI_F/dt=100A/μs	-	60	-	ns
Reverse Recovery Charge	Q_{rr}		-	150	-	nC

Fig 1. Typical Output Characteristics

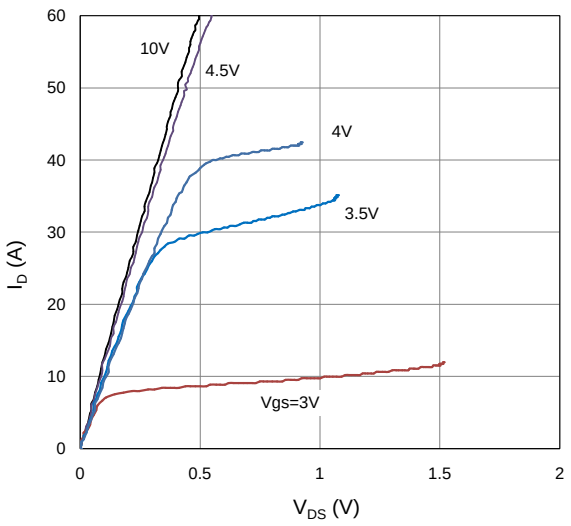


Figure 2. On-Resistance vs. Gate-Source Voltage

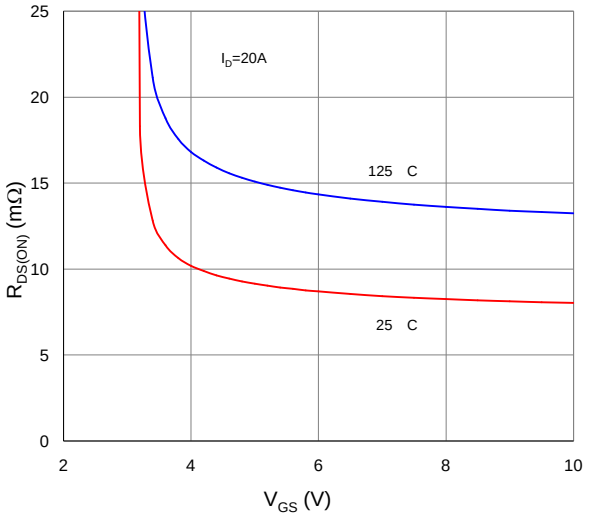


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

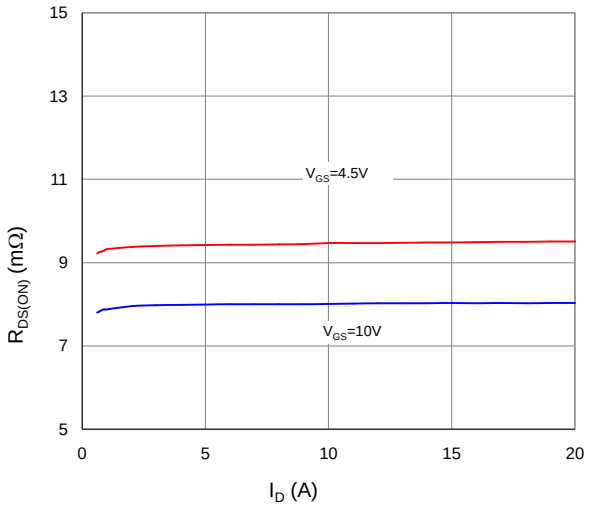


Figure 4. Normalized On-Resistance vs. Junction Temperature

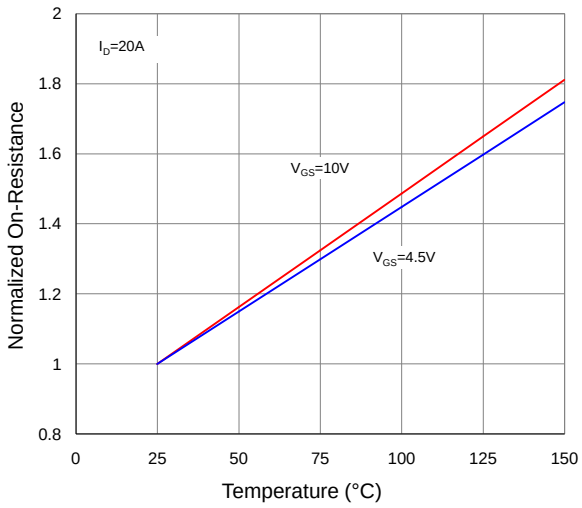


Figure 5. Typical Transfer Characteristics

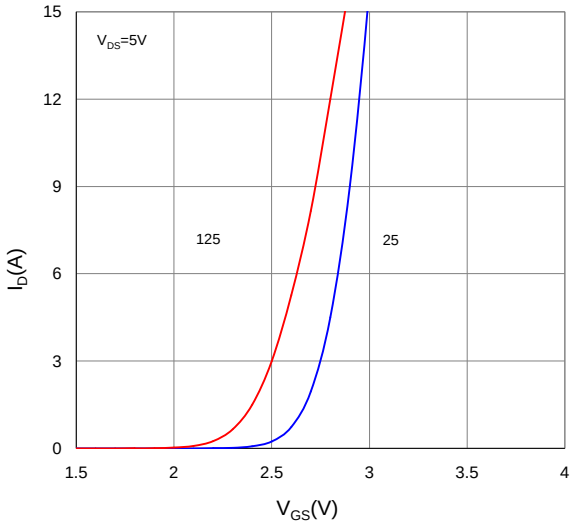


Figure 6. Typical Source-Drain Diode Forward Voltage

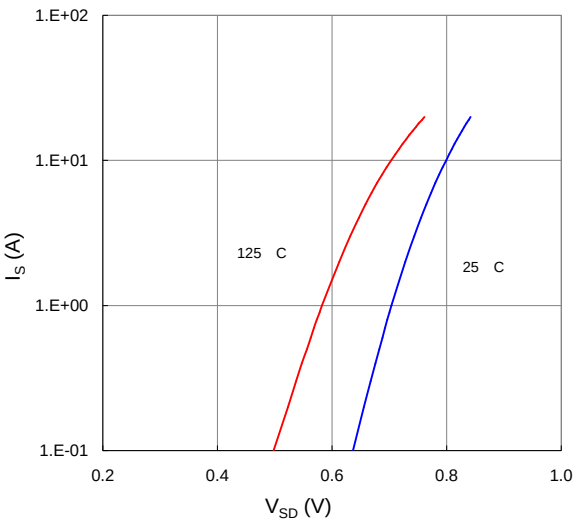


Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

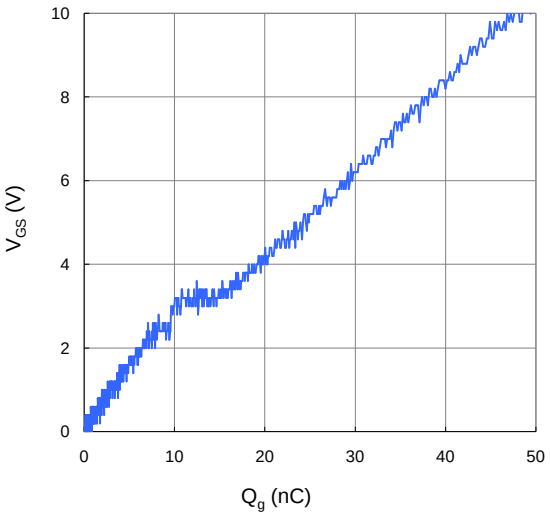


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

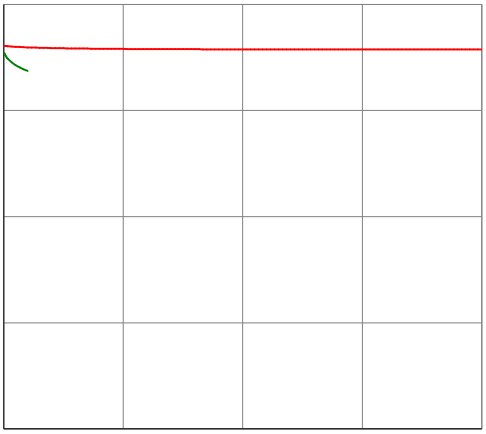


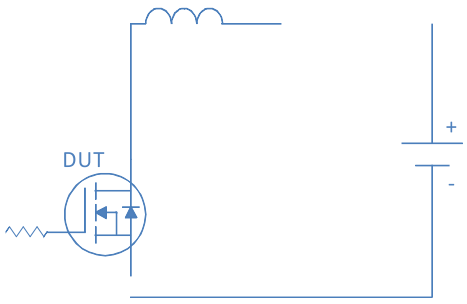
Figure 9. Maximum Safe Operating Area

Figure 10. Maximun Drain Current vs. Case Temperature

Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient

Inductive switching Test	

Gate Charge Test	

Uclamped Inductive Switching (UIS) Test	
	

Diode Recovery Test	

Package Outline

DFN5x6_P, 8 Leads

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A3	0.254 REF		0.010REF	
D	4.680	5.120	0.184	0.202
E	5.950	6.100	0.233	0.240
	0.162	D1	3.610	4.110	0.142
	0.149	E1	3.380	3.780	0.133
	0.197	D2	4.800	5.000	0.189
	0.229	E2	5.674	5.826	0.223
	0.055	k	1.100	1.390	0.043
	0.020	b	0.330	0.510	0.013
1.270TYP		e	1.270TYP		
	0.028	L	0.510	0.711	0.020
0.576	0.017	0.023	L1	0.424	
0.029		0.410		0.726	0.016
12°	0°	12°	θ	0°	12°