

45V N-Ch Power MOSFET

V_{DS}		45	V
$R_{DS(on),typ}$	$V_{GS}=10V$	3.8	m
$R_{DS(on),typ}$	$V_{GS}=4.5V$	5.3	m
I_D		20	A

Part Number	Package	Marking
HGS054NE4SL	SOIC-8	GS054NE4SL

Absolute Maximum Ratings at T_j

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current (Silicon Limited)	I_D	T_C	20	A
		T_C	12	
Drain to Source Voltage	V_{DS}	-	45	V
Gate to Source Voltage	V_{GS}	-	20	
Pulsed Drain Current	I_{DM}	-	80	
Avalanche Energy, Single Pulse	E_{AS}	$L=0.3mH, T_C$	60	mJ
Power Dissipation	P_D	T_C	3.1	
Operating and Storage Temperature	T_J, T_{stg}	-	-55 to150	

Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Lead	R_{JL}	23	
Thermal Resistance Junction-Ambient (steady state)	R_{JA}	40	
		75	

Electrical Characteristics at T_J
Static Characteristics

Parameter	Symbol	Test Conditions
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=20A$
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=20A$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS}=0V, V_{DS}=4.5V$
Gate to Source Leakage Current	I_{GSS}	$V_{GS}=10V, V_{DS}=4.5V$
Drain to Source on Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=20A$
Transconductance	g_{fs}	$V_{GS}=4.5V, I_D=20A$

Dynamic Characteristics

Input Capacitance	C_{iss}
Output Capacitance	C_{oss}
Reverse Transfer Capacitance	C_{rss}
Total Gate Charge	$Q_g(4.5V)$

Fig 1. Typical Output Characteristics



Figure 2. On-Resistance vs. Gate-Source Voltage

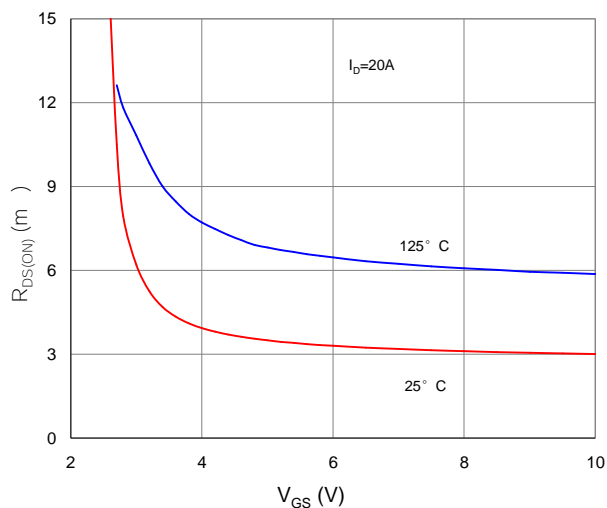


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

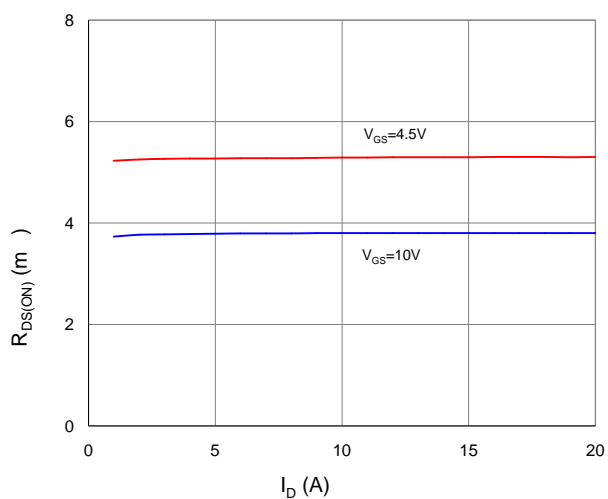


Figure 4. Normalized On-Resistance vs. Junction Temperature

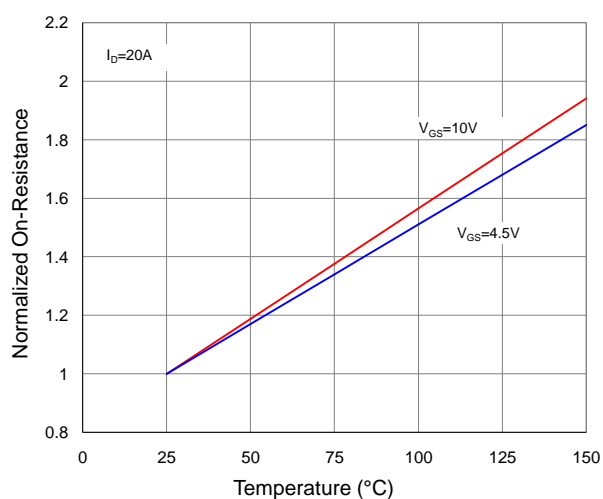


Figure 5. Typical Transfer Characteristics

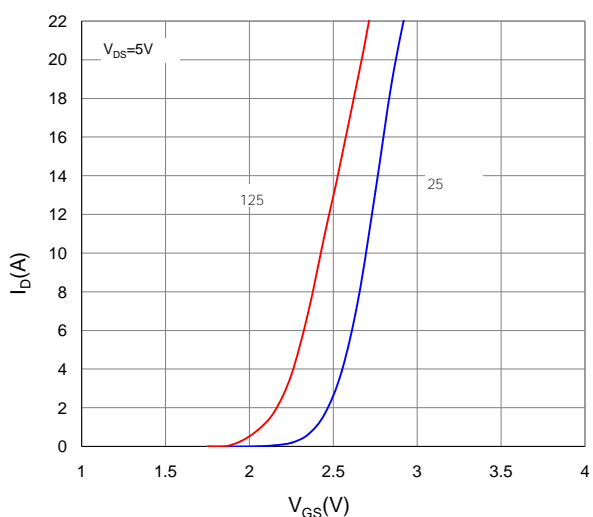


Figure 6. Typical Source-Drain Diode Forward Voltage

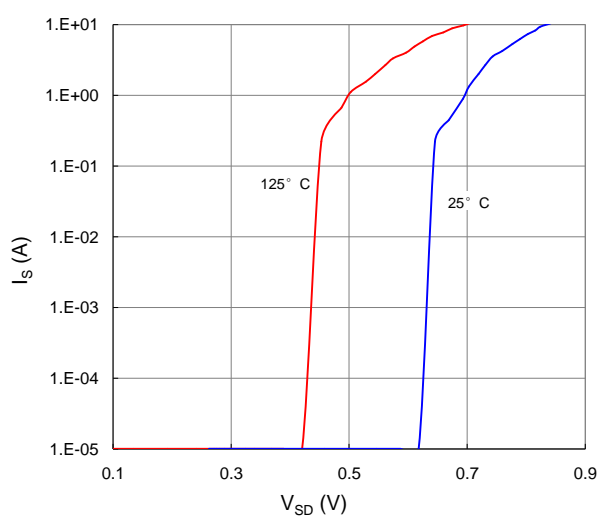


Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

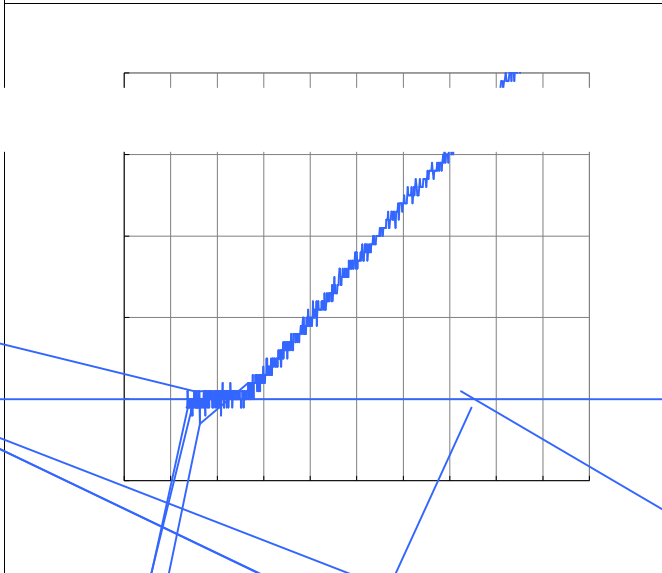


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

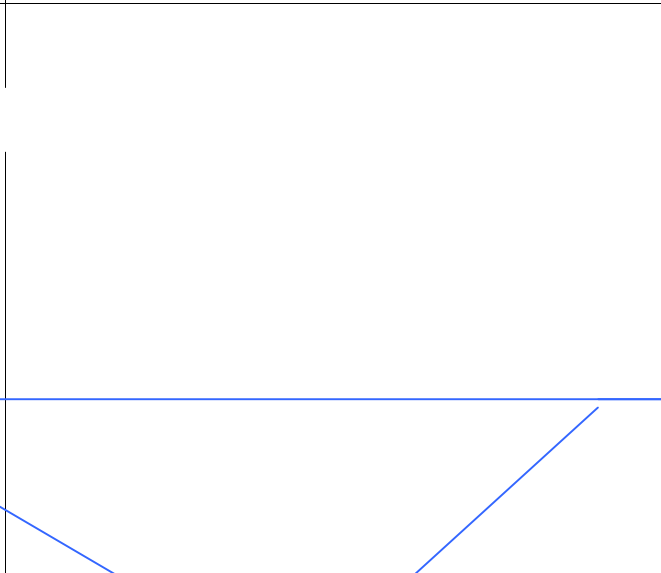


Figure 9. Maximum Safe Operating Area

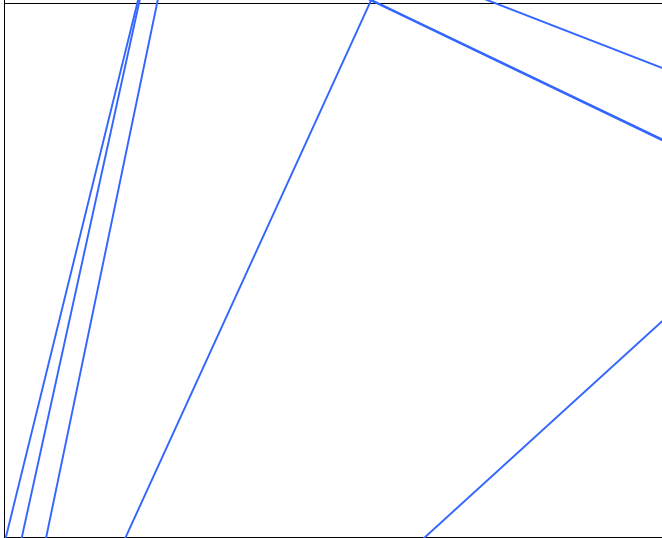


Figure 10. Maximum Drain Current vs. Case Temperature

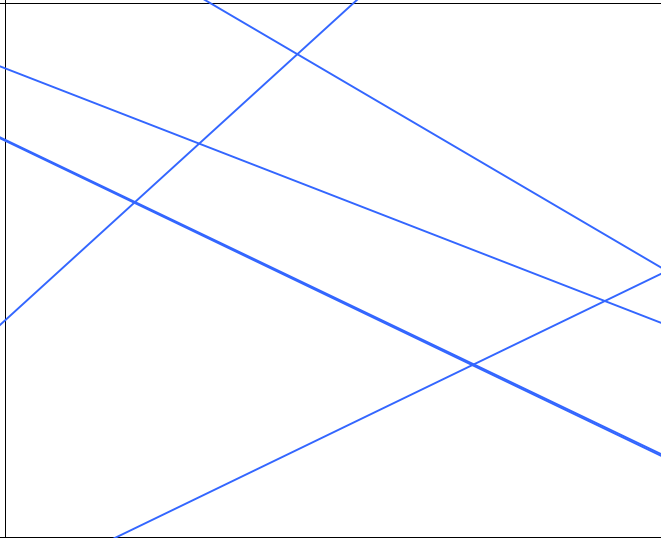
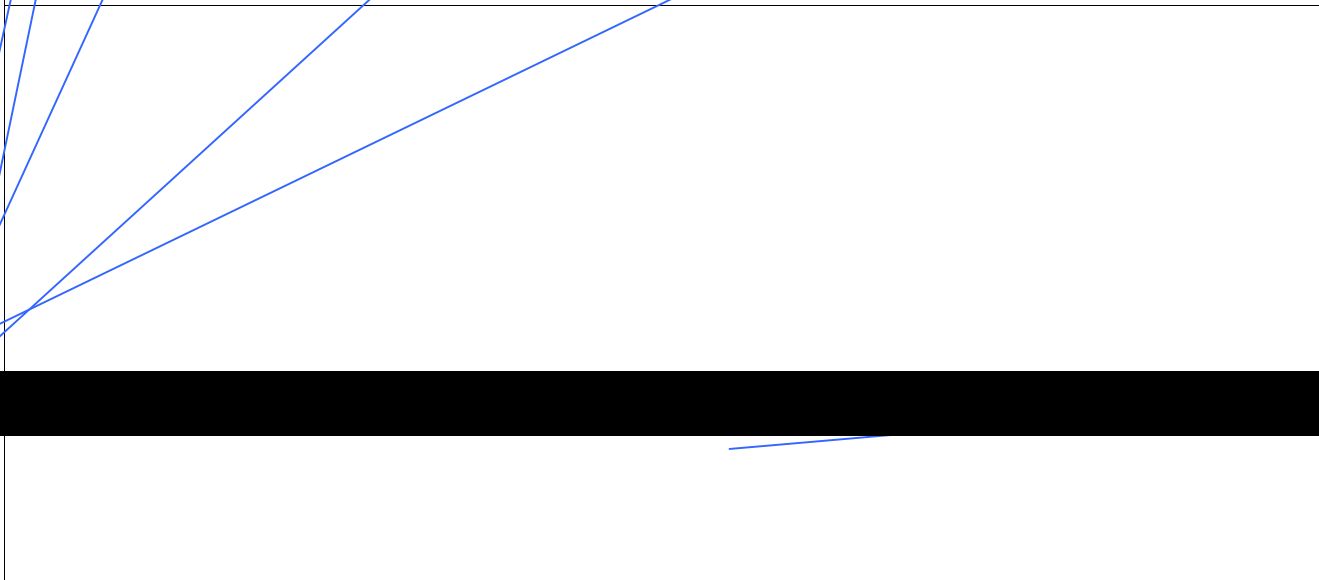
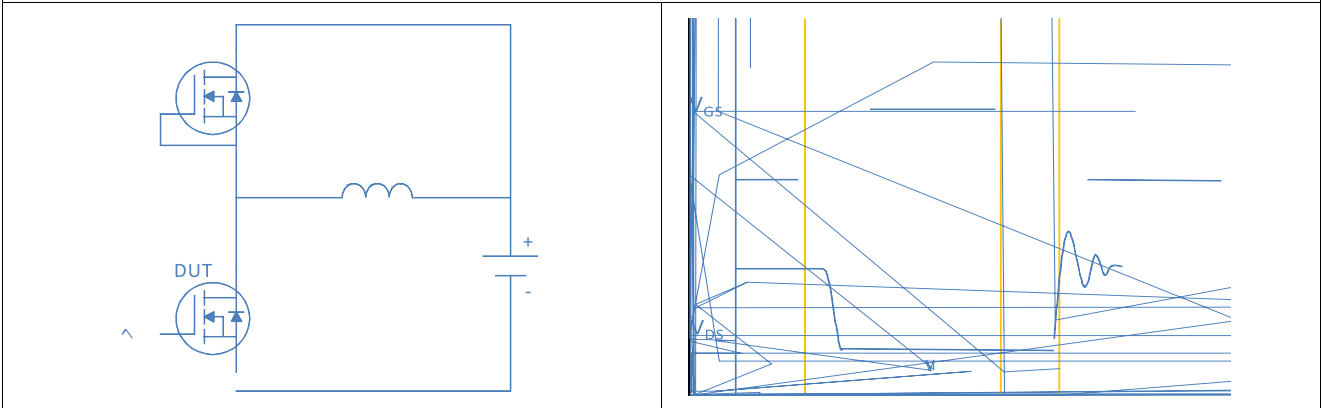


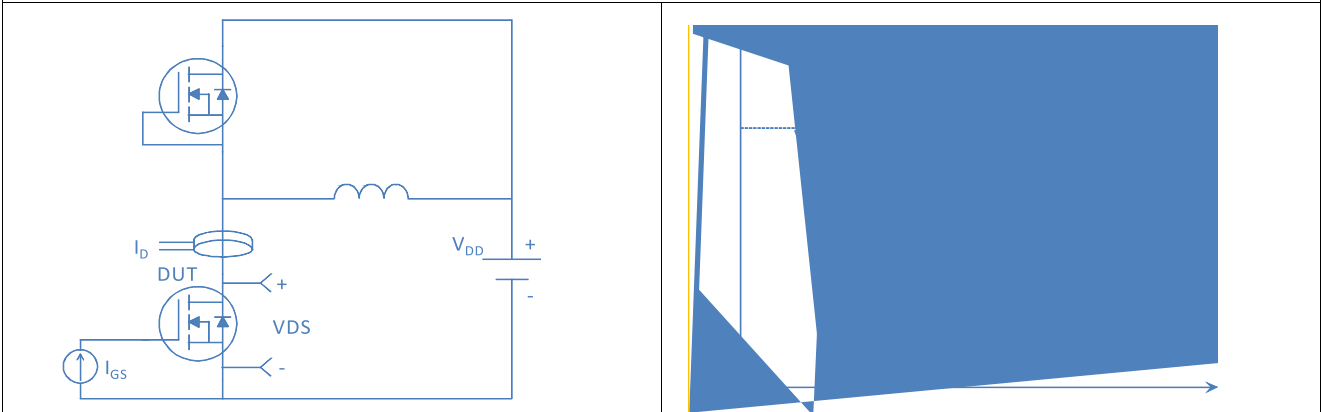
Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient



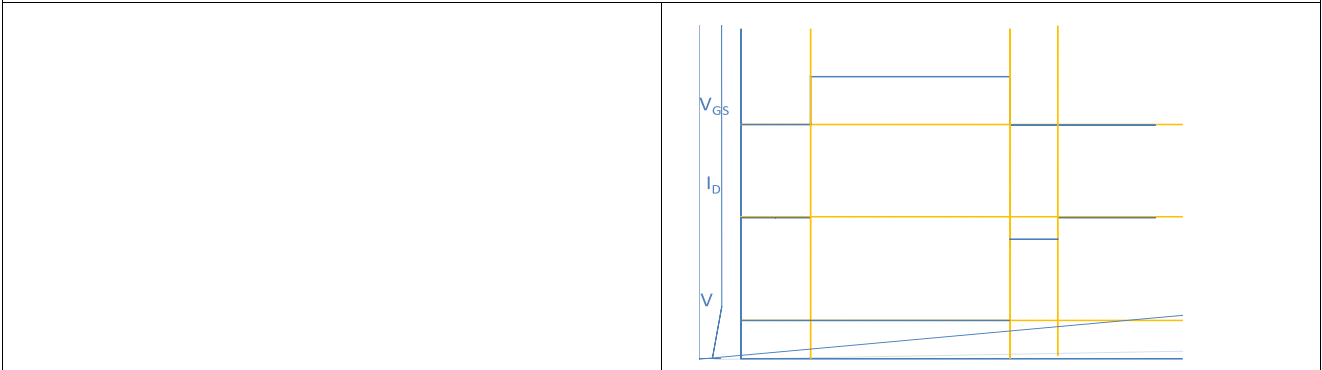
Inductive switching Test



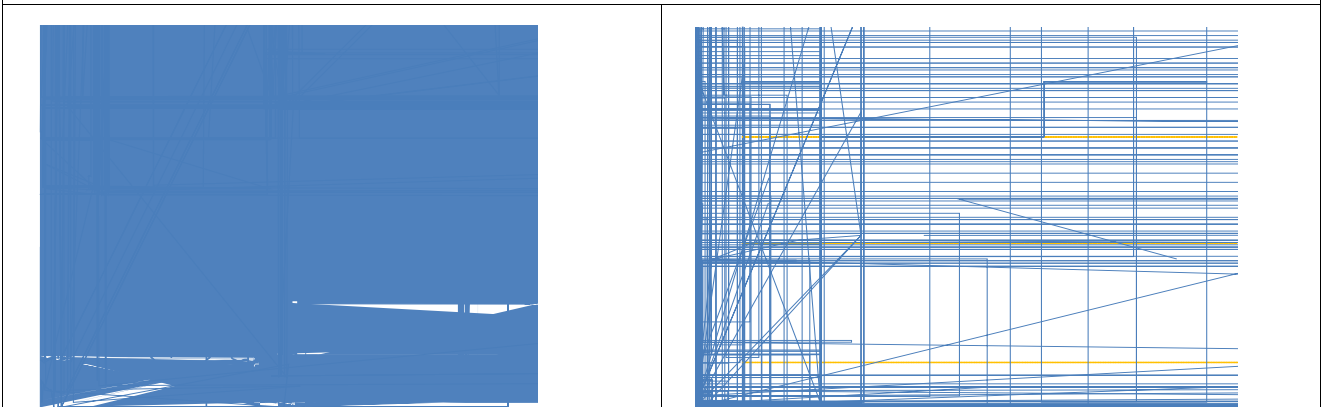
Gate Charge Test



Uclamped Inductive Switching (UIS) Test

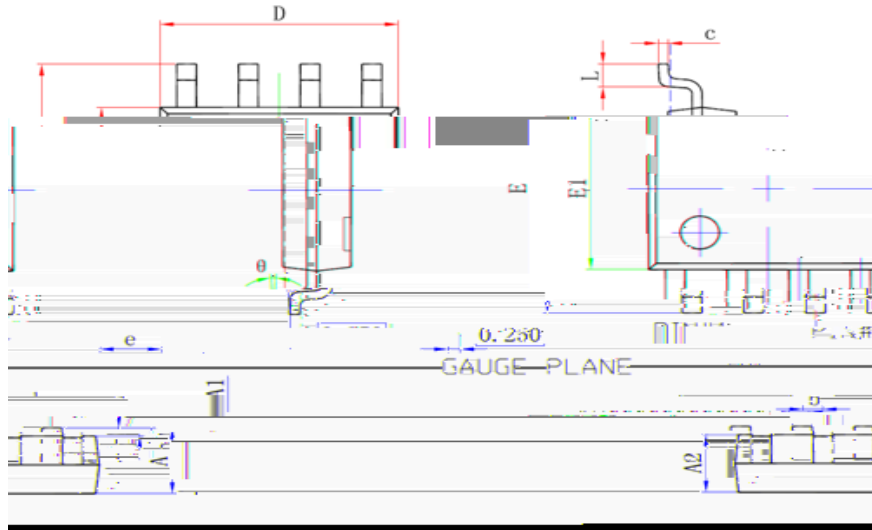


Diode Recovery Test



Package Outline

SOIC-8, 8 leads



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.250	1.650	0.049	0.065
b	0.310	0.510	0.012	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (SBC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.031
θ	0°	8°	0°	8°