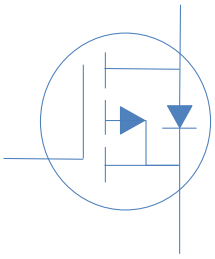
100V P-Ch Power MOSFET

V_{DS}		-100	V
$R_{DS(on),typ}$	V_{GS}=-10V	200	mΩ
$I_{D\ (Sillicon\ Limited)}$		-10	A



Part Number	Package	Marking
HTP2K1P10	TO-220	TP2K1P10

Absolute Maximum Ratings at T_j=25 (unless otherwise specified)

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current (Silicon Limited)	I_D	T_C=25	-10	A
		T_C=100	-7	
Drain to Source Voltage	V_{DS}	-	-100	V
Gate to Source Voltage	V_{GS}	-	±20	V
Pulsed Drain Current	I_{DM}	-	-40	A
Avalanche Energy, Single Pulse	E_{AS}	L=0.1mH, T_C=25	7.2	mJ
Power Dissipation	P_D	T_C=25	29	W
Operating and Storage Temperature	T_J, T_{stg}	-	-55 to 150	

Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Ambient (t≤10s)	$R_{\theta JA}$	62.5	/W
Thermal Resistance Junction-Case	$R_{\theta JC}$	4.3	/W

Electrical Characteristics at T_j=25 (unless otherwise specified)

Static Characteristics

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=-250μA	-100	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=-250μA	-1.0	-2.0	-3.0	
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS}=0V, V_{DS}=-80V, T_j=25	-	-	-1	μA
		V_{GS}=0V, V_{DS}=-70V, T_j=125	-	-	-25	
Gate to Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Drain to Source on Resistance	$R_{DS(on)}$	V_{GS}=-10V, I_D=-10A	-	200	250	mΩ
Transconductance	g_{fs}	V_{DS}=-5V, I_D=-10A	-	7	-	S
Gate Resistance	R_G	V_{GS}=15mV, V_{DS}=0V, f=1MHz	-	4.5	-	Ω

Dynamic Characteristics

Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=-25V, f=1MHz	-	2018	-	pF
Output Capacitance	C_{oss}		-	82	-	
Reverse Transfer Capacitance	C_{rss}		-	61	-	
Total Gate Charge	Q_g(10V)	V_{DD}=-80V, I_D=-10A, V_{GS}=-10V	-	31	-	nC
Gate to Source Charge	Q_{gs}		-	6.3	-	
Gate to Drain (Miller) Charge	Q_{gd}		-	4.5	-	
Turn on Delay Time	$t_{d(on)}$	V_{DD}=-10V, I_D=-1A, V_{GS}=-10V, R_G=6Ω,	-	12	-	ns
Rise time	t_r		-	55	-	
Turn off Delay Time	$t_{d(off)}$		-	40	-	
Fall Time	t_f		-	40	-	

Reverse Diode Characteristics

Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_F=-10A	-		1.3	V
Reverse Recovery Time	t_{rr}	I_F=-5A, dI_F/dt=100A/μs	-	70	-	ns
Reverse Recovery Charge	Q_{rr}		-	420	-	nC

Figure 3. On-Resistance vs. Drain Current and Gate Voltage

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

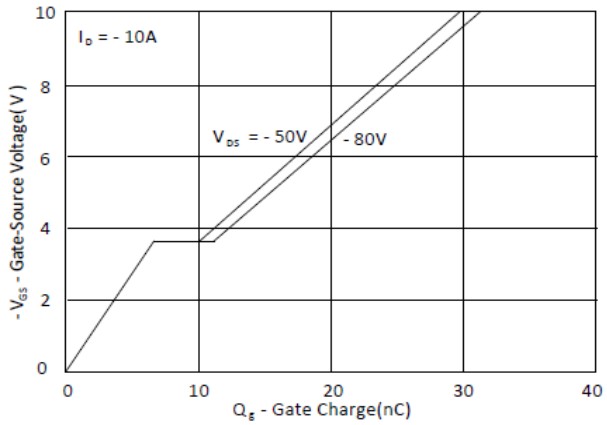


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

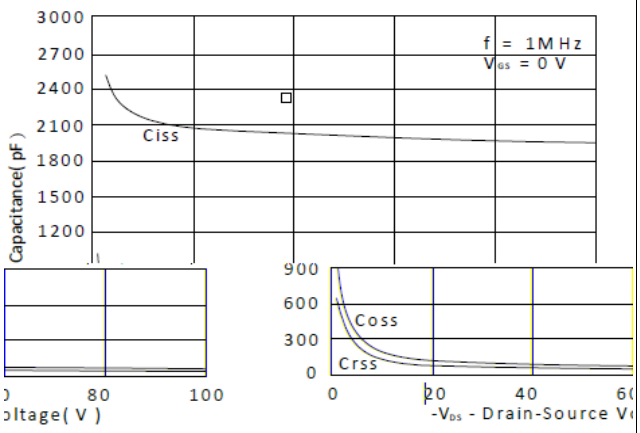


Figure 9. Maximum Safe Operating Area

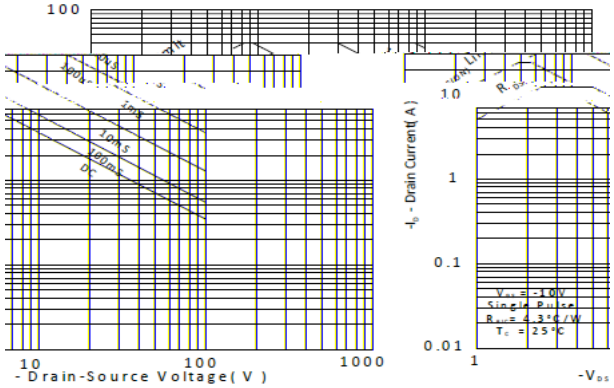


Figure 10. Single Pulse Maximum Power Dissipation

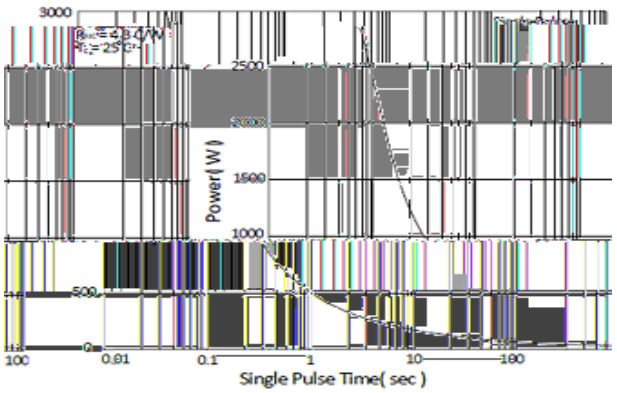
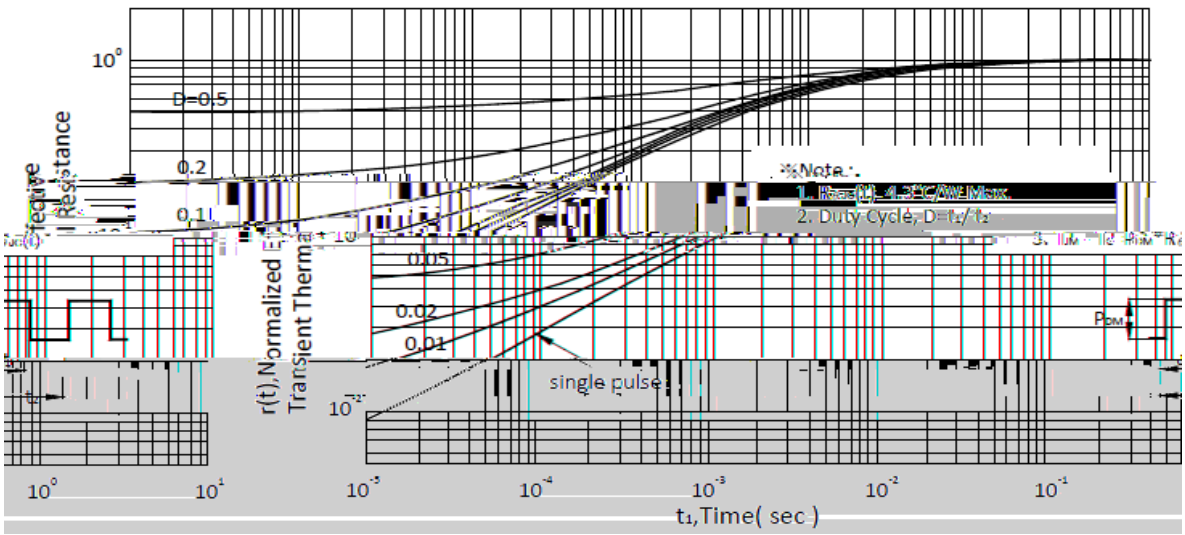
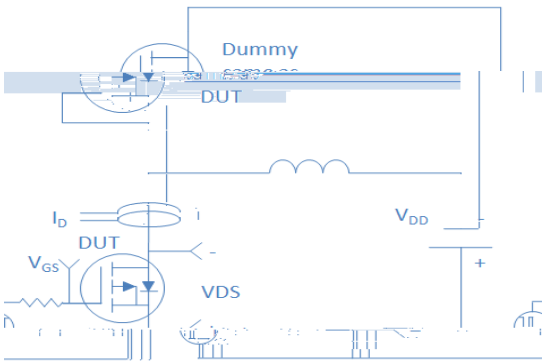
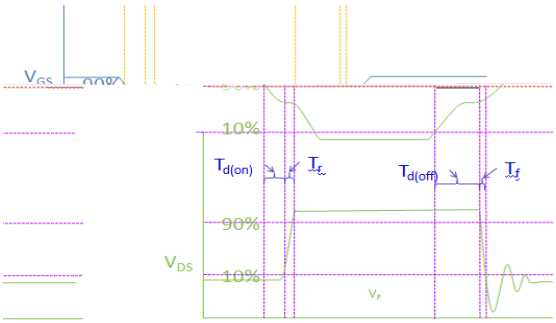


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient

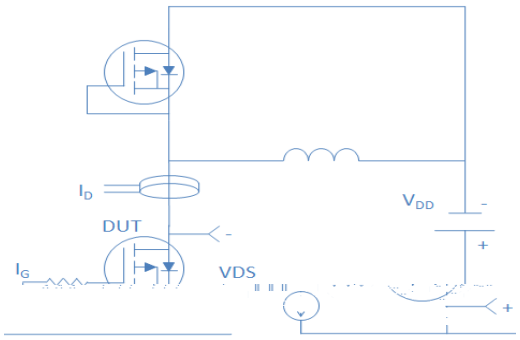


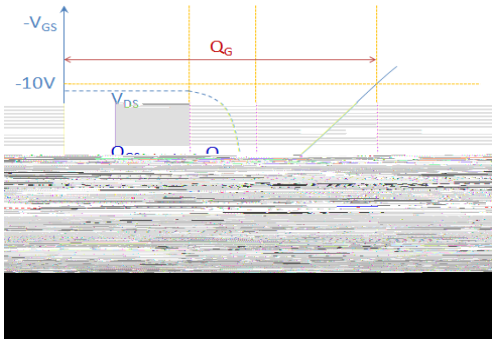
Inductive switching Test



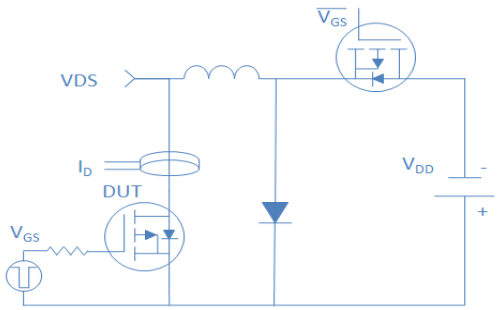


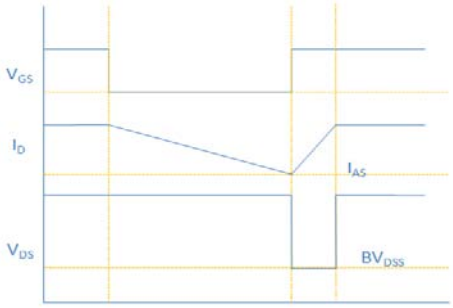
Gate Charge Test



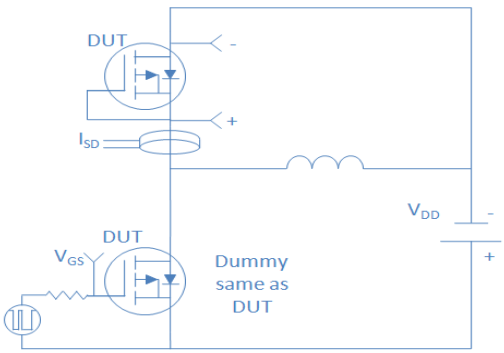


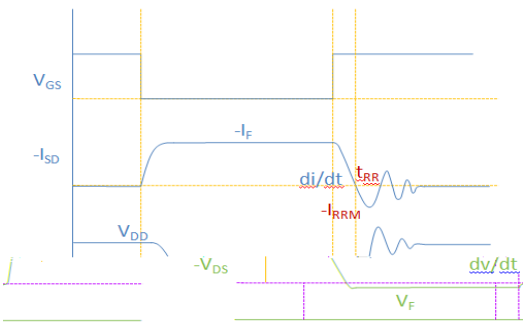
Uclamped Inductive Switching (UIS) Test





Diode Recovery Test





Package Outline

TO-220, 3 leads

Dimentions in mm unless otherwise specified

Symbol	Min	Nom	Max
A	9.66	9.97	10.28
A2	9.80	10.00	10.20
B	15.60	15.70	15.80
C	12.70	13.48	14.27
D	4.30	4.50	4.70
E	9.00	9.20	9.40
F		2.54	
G1	1.32	1.52	1.72
G2	0.70	0.82	0.95
G3	0.45	0.52	0.60
H	3.50	3.60	3.70
I	2.70	2.80	2.90
J	15.70	15.97	16.25
K	2.20	2.40	2.60
L	1.15	1.27	1.40
N	6.40	6.60	6.80